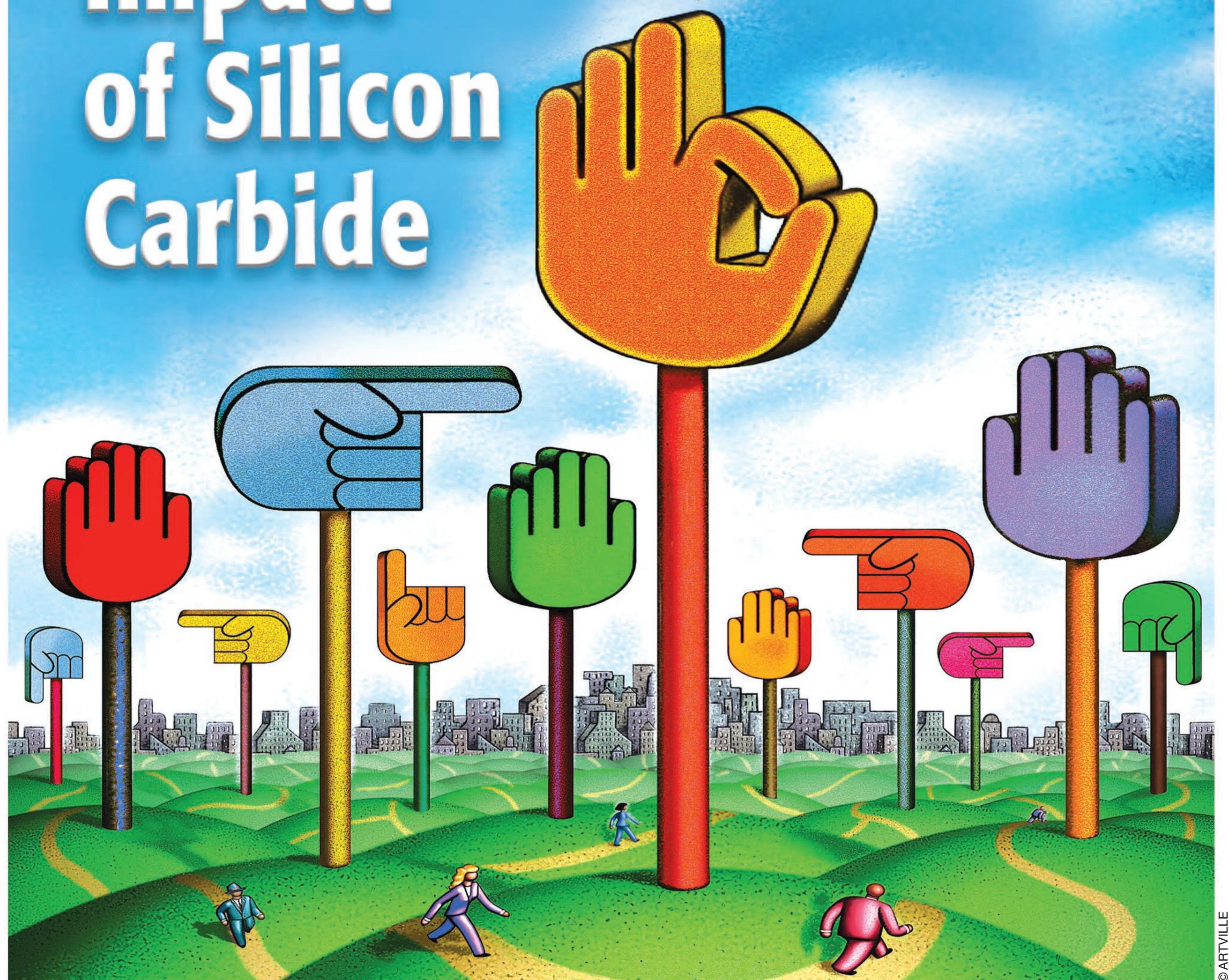

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Commercial Impact of Silicon Carbide

Opportunities and Challenges in Realizing the Full Potential of SiC Power Devices

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Evolutionary improvements in silicon (Si) power devices through better device designs, processing techniques, and material quality have led to great advancements in power systems in the last four decades. However, many commercial power devices are now approaching the theoretical performance limits offered by the Si material in terms of the capability to block high voltage, provide low on-state voltage drop, and switch at a high frequency. Therefore, in the past five to six years, many power system designers have been looking for alternative solutions in order to realize advanced commercial and military hardware that requires higher power density circuits and modules. One of the most promising approaches is to replace Si as the material of choice for fabrication of power devices with a wider bandgap

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material with acceptable bulk mobility [1]. A strong effort is now underway to exploit the excellent properties of silicon carbide (SiC) for the realization of high-performance, next-generation power devices. These material properties include: a) an order of magnitude higher breakdown electric field, b) a ~3X wider bandgap, and c) a ~3X higher thermal conductivity than Si. For a properly designed device, a high breakdown electric field allows the design of SiC power devices with thinner and higher doped blocking layers. The large bandgap of SiC results in a much higher operating temperature and higher radiation hardness. The high thermal conductivity for SiC (4.9 °C/W) allows dissipated heat to be more readily extracted from the device. Hence, a larger power can be processed with a device for a given junction temperature.

Power Applications and Devices

The use of more efficient power devices is expected to have a major impact on the energy use in the United States, which is estimated to be approximately 10^{14} BTUs. Approximately 27% of this is used for transportation, and 40% through direct use into electrical applications. By some estimates, hybrid vehicles may reduce the consumption of gasoline and result in saving US$16 billion worth of oil imports in the United States. In the United States today, approximately 15% of electricity is consumed in the info-tech industry, approximately 15% in lighting applications, 15% in heating and cooling applications, and another 55% in other motor control applications. For direct electric use, the voltage and current ratings of some major areas of electric power consumption are shown in Figure 1, with particular emphasis on some dominant areas of applications. Although the current and voltage ratings of power supplies are modest, they consume a large number of power semiconductor rectifiers and switches, while power transmission and distribution systems consume fewer power semiconductors but may provide a strong impact on system performance and reliability. By a rough estimation, motor control applications (including heating and cooling) consume approximately 60% of all electricity used in the United States, and lighting applications cover 15% of electric power.

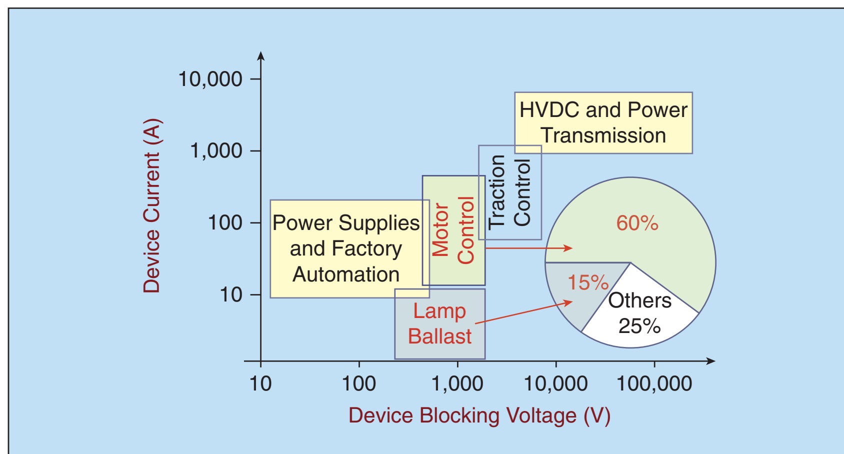

FIGURE 1 — Voltage and current ratings of various power applications.

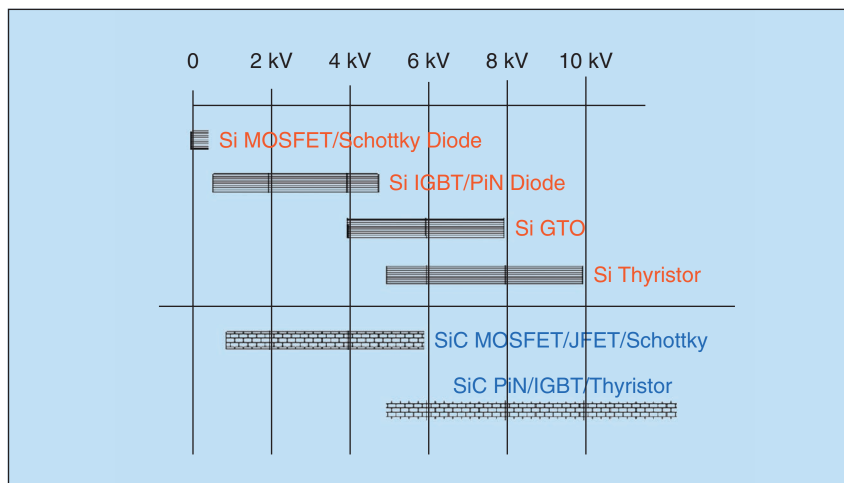

FIGURE 2 — Power device voltage ratings of Si versus SiC devices.

The ratings of commercial Si power devices where the bulk of these devices are used are shown in Figure 2. Most state-of-the-art power applications use power MOSFETs, p-i-n rectifiers, and insulated gate bipolar transistors (IGBTs) because the ratings of these devices are in the "sweet spot" of the power applications. Since SiC offers much lower on-resistance than Si, power MOSFETs and various flavors of Schottky diodes are considered promising candidates to replace Si power MOSFETs, Si IGBTs, and Si PiN rectifiers in the >600-V ratings. Apart from high ambient temperature applications like oil drilling, airborne applications, and high-radiation space applications, SiC devices may not offer any performance advantage as compared to Si devices in the commercially significant <600-V market. For applications that require >8-kV power semiconductors, bipolar SiC devices hold a strong promise.

As in Si, SiC power devices may be broadly classified into majority carrier devices, which primarily rely on drift current during on-state conduction; and minority carrier devices (also called bipolar-type devices), which result in conductivity modulation during on-state operation. Majority carrier devices like the Schottky diodes, power MOSFETs, and JFETs offer extremely low switching power losses because of their high switching speed. Although the on-state (forward) voltage drop of majority carrier devices can be low, it becomes prohibitively high at high current densities. This problem exponentially increases in its severity as the voltage rating on

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power devices is increased. On the other hand, bipolar-type devices such as p-i-n diodes, IGBTs, thyristors, bipolar junction transistors (BJTs), and field-controlled thyristors (FCTs) offer low forward voltage drops at high current densities but have higher switching losses than majority carrier devices. However, SiC bipolar devices suffer from a ~4X higher built-in junction voltage drop as compared to Si devices due to their larger bandgap resulting in a large forward voltage at low currents. Although the total on-state drop of SiC bipolar devices may be lower than Si devices in the ultra-high voltage regime, their full potential may be difficult to realize because conventional power device packaging technology can only dissipate 200–300 W/cm^2 continuously. Since the built-in voltage of 4H-SiC bipolar devices is ~2.8 V, the maximum continuous current may be limited to less than 100–150 A/cm^2 [2] for bipolar device types that have an odd number of p-n junctions (the built in potential can cancel in devices with an even number of junctions).

A strong effort is now underway to exploit the excellent properties of silicon carbide (SiC) for the realization of high-performance, next-generation power devices.

Numerous SiC majority carrier power devices that have recently been demonstrated break the "silicon theoretical limits" and have led to an acceleration of research and development activity. Probably the most exciting event establishing the viability of majority carrier SiC power devices is the commercial release of SiC Schottky rectifiers in the 600-V range [3]. On a 0.64-cm^2 single-chip SiC Schottky diode, a current of 130 A was demonstrated [4] using micropipe-free regions of a wafer. Junction barrier Schottky diodes with commercially attractive current capabilities have been demonstrated in the 1,200–2,800-V range [5]–[7] and may become the next commercial SiC device type. The power MOSFET in SiC is a relatively simple device type with excellent prospects as a candidate to improve and extend the capability of Si IGBTs in a wide range of applications. Even though the SiC MOS inversion layer mobility requires much research, important advances have been demonstrated in planar MOS devices. These include the demonstration of 10-kV power MOSFETs [8], [9] and accumulation-mode MOSFETs (ACCUFET) with a low specific on-resistance of 15 mΩcm^2 [10]. Another development in MOS-based power SiC FETs that has resulted in a device far exceeding the theoretical performance limitations of Si is the 5-kV SIAFET [11]. The SiC JFET is a majority carrier device type that does not suffer from the low MOS inversion channel mobility and high temperature gate oxide reliability challenges of the SiC MOSFETs. The highest voltage SiC-based JFET demonstrated in a practical circuit includes the 5.5-kV SEJFET [12]. Other JFETs with commercially relevant capabilities have been demonstrated with capabilities of 4 A at up to 3.3 kV [13]. To achieve low on-state resistance in JFETs, researchers have proposed to use a small positive bias on the gate electrode to aid the JFET channel conductance. Examples of such efforts are the 5-kV SIJFET [14], 600-V 10-A MOS-enhanced JFET [15], and the 1.7-kV JFET [16]. A novel approach proposed in the mid-1990s [17] exploits the high-voltage advantage of SiC-based JFETs and the mature fabrication technology and high channel mobility of a Si MOSFET in a cascode configuration. The net result is a hybrid device that offers the full functionality of a high-voltage power MOSFET [18].

On-state and switching design tradeoffs in bipolar devices are critically dependent on the stored charge. SiC bipolar devices have attracted much attention for high-power applications, because SiC bipolar devices have 30–100X less excess minority charge and tolerate a wide temperature excursion compared to Si bipolar devices with similar voltage ratings [19]. This is because: a) the voltage blocking layer is an order of magnitude thinner, b) the minority carrier lifetimes required for adequate conductivity modulation is much smaller, and c) the doping in the blocking layers are an order of magnitude higher than comparably rated Si devices. The highest voltage functional semiconductor device reported to date is the 19.3-kV SiC PiN rectifier [20]. After a long development process [19], the highest power single-chip SiC device (a PiN rectifier) was demonstrated recently with a 7.4-kV, 330-A (pulsed) capability [21]. Similar devices have been put in active circuits to show the benefits of SiC PiN rectifiers for utility applications [22]. Thyristors were among the first three-terminal bipolar switches that attracted reasonable attention because they can offer very high current density operation [23]. Recently, higher power gate turn-off thyristors (GTOs) have been demonstrated with 3–12-kV blocking capability [24], [25]. BJTs in SiC have become popular because of their low on-state voltage drop, ease of manufacture, and high yields. Devices with blocking capability of 1.8 kV, 10 A [26], and 3.1 kV [27] have been demonstrated with good current gains. Although many difficult technological issues must be solved before viable ultra-high-voltage SiC IGBTs can be commercialized, demonstration of 400-V, 2-A IGBTs operating at 400 °C [28] certainly show a promising start. FCTs offer excellent performance and ease of manufacture [29] in SiC but may require further refinements in materials and processing technology. Experimental demonstration of these 300-V, 1-A devices operating at 250 °C show the feasibility of this concept.

As a semiconductor material, SiC is projected to be superior for the realization of devices capable of operating at high temperatures as compared to contemporary devices. This is

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because SiC has a high "intrinsic temperature," defined as the temperature at which the intrinsic carrier concentration approaches the lowest doped region in the active power device. The intrinsic blocking voltage capability of a p-n junction made with a particular material is lost at this temperature. For a voltage blocking layer doping of 10^{16} cm^{-3}, this temperature is 1,320 °C for 4H-SiC, as compared to only 370 °C for Si. Although many researchers have demonstrated SiC devices operating at temperatures beyond the conventional range of up to 150–175 °C, the reliable long-term operation of these devices has not been proven. Some of these demonstrations in the past few years include: 100-V/1.2-A JFETs operating at 600 °C [30] for 30 h, 5-kV PiN diodes operating at 300 °C [4], MPS diodes operating at 250 °C [31], p-IGBTs operating at 400 °C [28], and 300-V FCTs operating at 250 °C [29]. While devices that rely primarily on the characteristics of PN junctions like PiN diodes, BJTs, and thyristors may not have physical limitations for high-temperature operation, MOS-based and Schottky metal-based devices do face some fundamental physics-based issues as described above.

Despite these promising demonstrations by many groups around the world, there are some issues faced by SiC still preventing it as a material of choice for commercial power devices. Although some of these issues reflect the relative immaturity of this technology, some may require years of development or may be fundamental to this new material system. As devices emerge that perform at temperatures exceeding theoretical limits of Si, new material and packaging reliability challenges will have to be addressed.

SiC Materials Issues

Most of SiC's superior intrinsic electrical properties have been known for decades. At the genesis of the semiconductor electronics era, SiC was considered an early transistor material candidate along with germanium and Si. However, reproducible wafers of reasonable consistency, size, quality, and availability are a prerequisite for commercial mass-production of semiconductor electronics. Many semiconductor materials can be melted and reproducibly recrystallized into large single crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all Si wafers, enabling reasonably large wafers to be mass-produced. However, because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional melt-growth techniques. This has prevented the realization of SiC crystals suitable for mass production. Prior to 1990, experimental SiC electronic devices were confined to small (typically $\sim$1 cm^2), irregularly shaped SiC crystal platelets grown as a byproduct of the Acheson process for manufacturing industrial abrasives (e.g., sandpaper) or by the Lely process. In the Lely process, SiC sublimed from polycrystalline SiC powder at temperatures near 2,500 °C are randomly condensed on the walls of a cavity forming small hexagonally shaped platelets. While these small, nonreproducible crystals permitted some basic SiC electronics research, they were clearly not suitable for semiconductor mass production. As such, Si became the dominant semiconductor fueling the solid-state technology revolution, while interest in SiC-based microelectronics remains limited mainly due to the lack of availability of high-quality SiC wafers. It is well known that SiC occurs in many polytypes in nature, with different bandgaps, carrier mobilities, and crystal structures. These polytypes are often found in many SiC crystals because it is difficult to control their growth.

The most commercially relevant SiC polytype (the 4H-SiC polytype) offers high breakdown electric fields ($>2 \times 10^6$ V/cm), high carrier mobilities, and relative maturity in wafer quality [32]. Currently, 4H-SiC wafers are commercially available in 2-in and 3-in diameter size only. Larger wafer sizes are necessary to reduce the device cost and enable the widespread adoption of SiC power devices, as exemplified by other semiconductor technologies. This is because only a handful of foundries that can handle such sized wafers remain in the world today. However, it is difficult to realize SiC wafers with a $>$4 in diameter because it is extremely difficult to control the temperature and growth rate during the realization of boules in SiC. In contrast to tens of feet of 12-in. Si boules grown commercially, SiC boules are limited to $<$50 mm and resemble a hockey puck. Despite this, SiC wafers are riddled with defects.

Material Defects in SiC

The most prominent defect in SiC is the micropipe, and many commercial wafers are graded according to this specification. A micropipe is a thermodynamically stable hollow core screw dislocation [32], which shows as a hole through a wafer within $\pm 15°$ off the c-axis of the wafer and is close to 1 μm diameter in size. It has been shown that an SiC device with a micropipe in its active area cannot support a significant electric field [32] and, hence, any significant power level. The micropipe densities in commercial wafers are steadily decreasing as material growth techniques mature, and currently it is possible to purchase wafers with a micropipe density of 5–10 cm^{-2}. However, it is imperative that this "killer defect" be eliminated in the future for the realization of high-current power devices.

Besides micropipes, there are many material defects commonly observed in present-day SiC, as shown in Figure 3. These defects can be broadly classified into wafer-level defects and epitaxial defects. Usually, SiC wafer defects act as nucleating sites for epitaxial defects that may affect device performance. Various defects on bare SiC wafers include the following:

- Closed core screw dislocation (with a typical 1,000–5,000 cm^{-2} density) is an ordered crystal defect, similar to a micropipe, that runs continuously over a significant thickness of the wafer. Depending on the epitaxial growth method, it may continue to grow into the epitaxial layers. If an active voltage blocking junction

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is formed on such a defect, a ~ 20% reduction in critical electric field can be observed [33]. These defects may result in a reduction in carrier lifetime of epitaxial layers grown over them [34].

- Basal plane dislocations (typical density: 10^2–10^5 cm^{-2}) are islands of single-crystal SiC with a displaced basal plane that may be annealed using advanced epitaxial growth techniques [34].
- Edge dislocations (10^4–10^5 cm^{-2}) are usually one-dimensional defects on the surface of wafers.
- Low-angle boundaries (10^2–10^3 cm^{-2}) and polishing damage found in commercial wafers result in increased leakage currents during reverse-bias operation of the these devices.

Defects in SiC epitaxial layers depend on the methods and reactors used to grow the layers. The most common epitaxial defects are growth pits (1–100 cm^{-2}), triangular inclusions of different polytype (e.g., 3C in 4H), carrot (0.1–10 cm^{-2}), and comet tail defects [35], as shown in Table 1. Growth pits and carrot defects result from wafer defects that create adverse conditions for the realization of a perfect crystal structure during epitaxial growth. Temperature nonuniformities during epitaxial growth cause the appearance of triangle inclusions of different polytypes. Poor management of impurities or premature nucleations of SiC particulates cause the formation of comet tails and other defects.

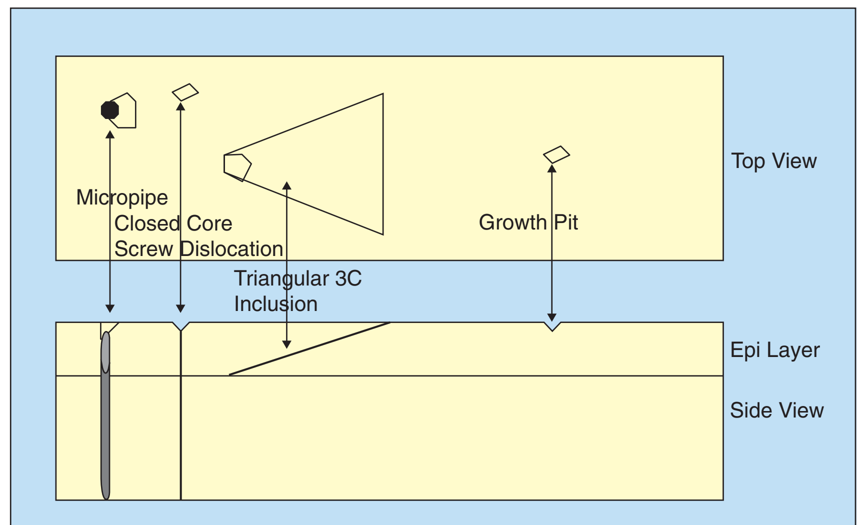

FIGURE 3 — Common material defects in SiC.

Reverse Characteristics of SiC Devices

When devices are in the reverse-blocking mode, i.e., reverse-biased Schottky and PN junctions, devices are expected to have low leakage current and have near-theoretical blocking voltage. From a reliability perspective, it is important to understand the effect of materials and processing defects on leakage current, total blocking voltage achieved, and sustainable avalanche energy achievable during breakdown. The effect of material defects on the device blocking performance has been discussed extensively by Neudeck et al. [34] and Kimoto et al. [35]. The most extensively studied defect in SiC is the screw dislocation [36]. Screw dislocations in PN diodes result in a higher leakage current, a softer breakdown of I-V characteristics, and cause the breakdown microplasma to concentrate through this defect. Although the leakage current mechanism is dominated by this defect, measurements over a 298–673 K temperature range show that the leakage current is tolerable in diodes with screw dislocations. The leakage current near avalanche breakdown voltage is similar in diodes with and without screw dislocations. In fact, a peak avalanche power density of 140 kW/cm^2 was applied in diodes with screw dislocations with repeatable reverse I-V characteristics. This indicates that a screw dislocation does not cause severe reduction in blocking voltage of power devices fabricated on them.

Schottky devices (e.g., power Schottky diodes and MESFETs) are very sensitive to surface and morphological defects. Even small areas with material defects that cause reduced metal-semiconductor barrier height can dominate reverse blocking characteristics [37]. This is because leakage currents in Schottky contacts are exponentially dependent on barrier height. Epitaxial growth, which is the main cause of morphological defects, is a much more important process for reliable and high yielding Schottky devices as compared to PN diodes. However, triangular 3C inclusions are quite devastating for blocking properties of both PN and Schottky devices. They result in >50% reduction in blocking voltage [34]. Carrots and comet tails result in some increase in leakage currents but do not cause a severe reduction in blocking voltage. Small growth pits seem to affect

TABLE 1—TYPICAL MATERIALS DEFECTS AND THEIR IMPACT ON DEVICES.

DEFECT TYPE	TYPICAL DENSITIES	AFFECT ON DEVICES
Micropipes	1–15 cm^{-2}	<50% E_{cr}
Carrots	0.1–10 cm^{-2}	E_{cr}, J_L, n
Mator pits	1–100 cm^{-2}	E_{cr}, J_L
Screw dislocation	10^3 cm^{-2}	<80% E_{cr}
Edge dislocation	10^4–10^5 cm^{-2}	??
Low angle grain bound	10^2–10^3 cm^{-2}	τ-reduction, forward chars
Stacking faults	1–100 cm^{-2}	τ-reduction

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Schottky diodes more severely than PN junction devices [34]. With the improvement of epitaxial processing these effects may be minimized for most SiC power devices.

Avalanche Energy

The pulsed avalanche energy is the amount of energy that the power device can handle safely while it is undergoing avalanche breakdown. This energy is determined by the adiabatic heating of the blocking layer and the intrinsic temperature of this low-doped SiC layer. The static avalanche power density of a PN junction made using a particular material depends on its density, specific heat, and the temperature at which the intrinsic carrier density becomes close to the doping density of the voltage blocking layers (i.e., the bandgap of the material). Theoretically, the total avalanche energy is calculated to be more than 10X higher than Si devices [38]. However, the breakdown current can become dominant over small filaments where all the breakdown microplasma is concentrated. This is true for both Si and SiC devices, and, usually, material defects in voltage blocking junctions initiate these microplasmas. Experimental results on SiC PN diodes fabricated show that approximately 5X higher avalanche energy was obtained as compared to Si PN devices in steady state [39].

Blocking Stability Demonstrations

Early indications of biasing SiC PN junction devices to their avalanche breakdown limits indicated that SiC devices may have a negative temperature coefficient of avalanche breakdown value [38]. However, later experimental results conclusively disproved these early observations [40]. Although the cause of the observed negative coefficient of avalanche breakdown was never conclusively determined, a hypothesis pointed to the role of crystal defects in this phenomenon. It is possible that poor process fabrication conditions resulted in surface contamination or surface states, which led to these unstable blocking characteristics of SiC diodes.

With the rapid introduction of commercial power devices, close attention is being paid to the reliability of power devices under all conditions. The material defects like micropipes are the primary yield-limiting factor for these devices. The first reported reliability testing on SiC Schottky diodes was made in 1999 by Rupp et al. [41]. In this study, 100 devices with 600-V rating were tested for a) thermal cycling up to 400 °C, b) cycling between −55 °C and 150 °C for 1,000 times, c) high-temperature reverse bias at 150 °C with a reverse bias of 600 V for 1,000 h, and d) high-humidity, high-temperature reverse-bias testing (85 °C, 85% relative humidity) for 1,000 h. None of these tests resulted in any failures. The yield on 600-V, 6-A Schottky diodes exceeded 75% in this report. Recently, another group [42] has also shown a total of 145,000 device hours of high-temperature reverse-bias testing, 11,000 device hours of continuous current "burn-in" testing, and 35,000 device hours of power cycling testing with no failures.

In a statistically significant study, higher voltage (3.2–4.0 kV) packaged PiN diodes were biased at 2,250 V under high temperatures (125 °C) for 500 hours [33] without showing catastrophic failure. In these devices, the leakage current remained in the 10^{-8}–10^{-4} A/cm^2 range. It is worthwhile to note that, in this study, many devices had a widely varying (factor of 10^4) level of leakage currents but remained stable with time and temperature. Although a few diodes showed sporadic increases in leakage currents, the total leakage current remained below the 10^{-4} A/cm^2 range. Many of these variations in leakage currents and their sporadic increases were probably caused by material and processing defects/variations.

These demonstrations have proven that although materials defects may cause limitations to yield and device performance in the blocking state, they do not result in severe long-term issues with respect to their blocking reliability and stability. These observed experiments are true for both PN and Schottky junction devices.

Forward Voltage Degradation in SiC PN Diodes

While the reverse-bias operation of SiC devices has been found to be relatively stable, a curious phenomenon observed recently during the forward-bias operation of SiC PiN diodes has caused a great deal of concern toward long-term stability of these devices. It has been observed that as PN diodes are forward biased for an appreciable length of time, their on-state voltage drop increases with time, as shown in Figure 4. The duration over which these devices show this forward-bias degradation varies from a few milliseconds

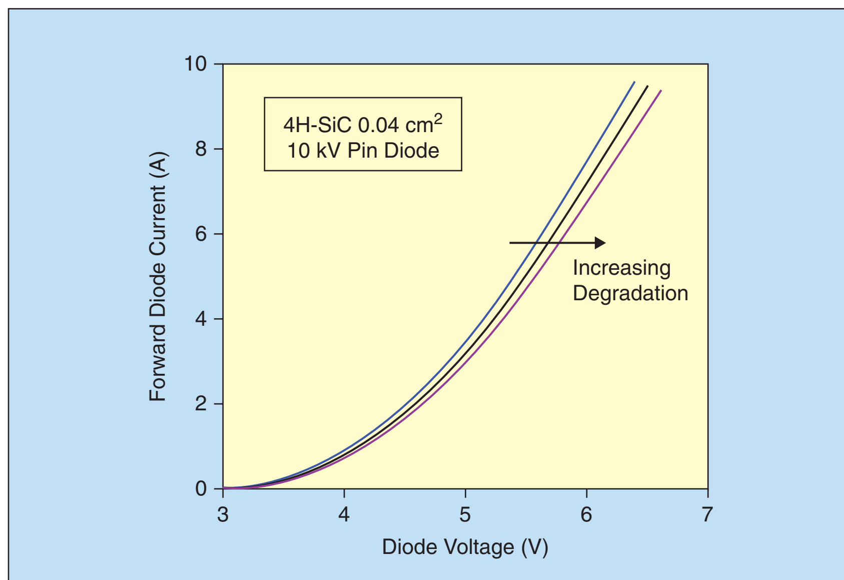

FIGURE 4 — On-state characteristics of a high-voltage SiC PiN diode after various levels of forward-bias stress.

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to many hours [43]. A variation in on-state voltage drop (V_F) in PiN diodes has serious stability concerns because it can result in current filamentation and local current "hogging." If a portion of the diode has a lower on-state voltage drop than another region within the same diode due to slight differences in material and processing variations, current will be diverted into the lower V_F region. This can cause excessive current densities in small portions of the diode, while leaving large portions of it with a low-current density, leading to thermal instability of the entire diode. Such characteristics will also prevent safe paralleling of devices to boost the total current required for typical high-current applications for which these devices are targeted.

With the rapid introduction of commercial power devices, close attention is being paid to the reliability of power devices under all conditions.

SiC Device Fabrication and Reliability

This section is focused on unique issues relating to SiC device fabrication and reliability. As is well known, SiC power devices are not fabricated in large-scale semiconductor foundries because they require unusual fabrication steps not suitable for adoption on an industrial scale. However, certain performance/reliability tradeoff issues related to Schottky diodes and SiC MOS-based devices may not be as widely known.

Unique SiC Fabrication Toolset

Fabrication of SiC devices is still immature as compared to those of other commercial semiconductors. The high thermal and chemical stability of SiC makes certain types of fabrication operations difficult. Issues that require particular attention are ion implantation, thermal oxidation, and ohmic contacts in SiC.

Insertion of n-type and p-type impurities into SiC is difficult because diffusion coefficients for dopant atoms are extremely low at the temperatures typically used for Si device processing; and, for this reason, selective doping of SiC is accomplished by ion implantation. In contrast to Si devices, which show good dopant insertion through room-temperature ion implants, SiC requires ion implantation to be accomplished at higher temperatures. This is difficult because the stage used to mount wafers during ion implants needs to be modified drastically to accommodate SiC wafers. It is difficult to convert conventional ion implant manufacturers to modify wafer end stages to make this change because it reduces the throughput of their tools, and this modification results in large uncertainties in the measurement of implant dose. Even after ion implantation at such high temperatures, most dopant species (like nitrogen and aluminum) create severe damage in SiC crystal because significantly high energy implants are required for even a modest implant range of 0.5 μm, as shown in Figure 5. Therefore, a post-implant anneal at $>$1,550 °C must be conducted to alleviate part of the crystal damage and increase the dopant incorporation into the crystal. Unfortunately, at such high temperatures, SiC disassociates and a significant loss of Si occurs from the SiC crystal. Therefore, ion implantation, dopant activation, surface integrity, and high-temperature annealing in SiC remains an important field of research and has not reached commercially acceptable standards. This is also an important capital expenditure required for any entity considering an endeavor into manufacturing SiC devices because an overwhelming majority of devices require ion implantation in their fabrication sequence.

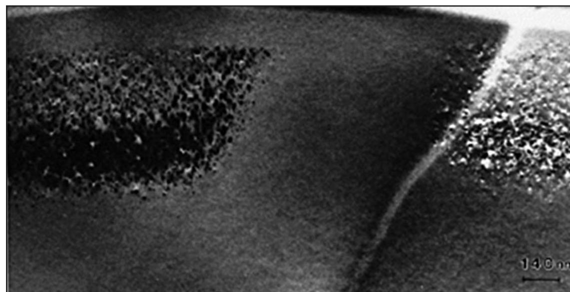

FIGURE 5 — Cross-sectional transmission electron microscope image of ion-implanted region in SiC shows significant carbon and dopant precipitation within the crystal.

Another fabrication aspect that requires significant attention is thermal oxidation of SiC. Because of the high bonding strength of Si and C in SiC, thermal oxidation rates are ~10X lower than Si. Therefore, temperatures in excess of 1,200 °C are routinely needed during fabrication of SiC devices. This temperature is beyond the temperature limit of most oxidation furnaces used in Si foundries because these furnaces are made of quartz, which softens close to this temperature. Modifications that prevent "sagging" of quartz tubes are required on this expensive piece of equipment.

In contrast to Si, chemical etching of SiC is impractical owing to the high chemical stability of SiC. Selective etching must be accomplished by reactive ion etching (RIE) using fluorinated gasses that produce severe damage on the etched surfaces. Even after this abrasive process, SiC may be etched only to modest depths of $\sim$1 μm. The wide bandgap of SiC makes it difficult for metals to form ohmic contacts with SiC because the electron affinity of most metals does not match the conduction band or the valence band of SiC. In contrast to Si, where ohmic contacts may be formed through room temperature deposition of suitable metal on Si, a high temperature annealing step is required in SiC after deposition of metals on the SiC surface to form a silicide between the metal and SiC. Often, this temperature may be in excess of 900 °C, which results in poor SiC–SiO_2 interface properties after this silicidation step.

While these factors pose challenges in the fabrication of SiC devices and limit the types of device structures that can be

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Probably the most exciting event establishing the viability of majority carrier SiC power devices is the commercial release of SiC Schottky rectifiers in the 600-V range.

realized in this material, there are certain fundamental reliability challenges faced by SiC devices as well. These are explained in the following sections.

Schottky Metal-Based Devices

In principle, while the reverse-leakage current of PN junction-based devices is largely determined by the bandgap of the semiconductor used, the reverse-leakage current for Schottky junctions that is expected to block the rated voltage is dependent on the metal-semiconductor barrier height. In some of the most-promising SiC-based power and microwave devices (the power Schottky diode and the microwave MESFET), a Schottky junction is required to block the rated voltage. To the first order, the leakage current in the Schottky diodes is given by [44]:

$$J_L = A^{**} T^2 \exp\left(-\frac{\Phi_{Bn}}{V_T}\right),$$

where A^{**} is the modified Richardson constant, T is the operating temperature, Φ_{Bn} is the metal-semiconductor barrier height, and V_T is the thermal voltage. This equation shows that the leakage current in a voltage-blocking Schottky junction is exponentially dependent on the metal-semiconductor barrier height and the operating temperature. Since SiC power Schottky diodes are expected to compete with Si PiN diodes, they must have a comparable forward on-state voltage drop. The most commonly used Schottky metals (e.g., titanium and nickel) have Φ_{Bn} values close to the Si bandgap value of 1.1 eV [45]. The high-temperature blocking performance of these Schottky diodes will only approach that on Si PiN diodes, which is in the 125–175 °C range, and not the 250–350 °C range promised for many PN junction based devices. The metal-Schottky barrier height is further reduced due to the effect of barrier height lowering when a high reverse electric field is present at the metal-SiC interface during blocking [45]. The presence of material defects also increases the leakage current in SiC Schottky diodes because these defects act as sites with lower Schottky barrier heights as compared to the bulk of the device [37]. Since the leakage current is exponentially dependent on the Schottky barrier height, even small areas with low Schottky barrier heights will contribute a significant portion of the leakage current and will be even more severely influenced by increasing temperature than if a uniform Schottky contact is assumed [37].

Fowler-Nordheim Tunneling

A natural oxide for SiC was considered a significant advantage for SiC as compared to other compound semiconductor materials since it enables the realization of the ideal switch in SiC, the power MOSFET, for a wide variety of applications. However, some fundamental physics-based issues and technological development issues have prevented the realization of the full commercial potential of a MOS-based SiC power device, despite decade long research on this device. A serious physics-based reliability challenge results from carrier tunneling into dielectrics. The most commonly cited intrinsic oxide degradation mechanism in SiC is the Fowler-Nordheim (FN) tunneling [32]. Metal-dielectric-semiconductor-based devices under high electric fields can suffer from a serious long-term reliability concern due to the FN tunneling current [32], [47]. The electric field in the dielectric results in an emission of carriers from the semiconductor into the dielectric, or from the gate metal into the dielectric, resulting in time-dependent dielectric breakdown (TDDB). Such a breakdown occurs over a finite period of time (depending on the electric field, temperature, and the band offsets) and manifests itself with an increasing leakage current between the gate metal and the semiconductor. The tunneling emission current is of the form [47]:

$$J^0_{F-N} = A.E^2 \exp\left(-\frac{B}{E}\right),$$

where J^0_{F-N} is the tunneling emission current at zero temperature, E is the electric field in the dielectric, and A and B are dependent on the properties of the relevant junction. The barrier height (Φ_B) is defined as the difference between the electron affinities of the metal/semiconductor and the dielectric. A and B have the following dependence on band offset:

$$A \propto \frac{1}{\Phi_B}$$

$$B \propto (\Phi_B)^{3/2}.$$

Note that the tunneling current emission is *exponentially dependent* on both the electric field in the dielectric and the barrier height. The temperature dependence of FN tunneling is too complicated to be treated in this article and is treated in detail by Pananakakis et al. [47]. To the first order, the FN current can be assumed to be proportional to the square of the temperature.

MOS in Forward Bias

Forward bias is defined to be when an NMOS device has a positive bias on the gate with respect to the source, or when a PMOS device has a negative bias with respect to the source. Most of the discussion here is concentrated on the NMOS case, while a similar parallel exists for the PMOS case. The barrier height for the purposes of FN tunneling is calculated as the difference between the conduction band of the dielectric and the Fermi level of the semiconductor. In the worst-case scenario for an NMOSFET, the Fermi level may be assumed to lie at the conduction band edge, which corresponds to a very strong inversion case, or when highly doped N-type SiC is used. For

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this condition, the barrier height for FN tunneling is the conduction band offset (electron affinity difference) between SiC and the dielectric. The following discussion will assume SiO_2 as the dielectric. FN tunneling currents are expected to be much higher at a given temperature and electric field for SiC-based devices than for Si based devices because the conduction band offset between SiC and SiO_2 is smaller than that between Si and SiO_2. As shown in Figure 6, the conduction band offset in the Si-SiO_2 interface is 3.2 eV, but it is only 2.7 eV for 4H-SiC. For a similar FN tunneling current, this 0.5 eV difference in the band offset will require that the electric field in the dielectric for an 4H-SiC/SiO_2 system be reduced by approximately 1.5X as compared to an Si/SiO_2 system.

In commercial Si NMOSFETs, the electric field in SiO_2 is kept below 4–5 MV/cm, so that a reasonable ten-year life is achieved [48]. Tunneling is the primary device-lifetime limiting factor for Si MOS based devices and is rated only to a maximum temperature of 125°C. Reducing the electric field in the dielectric to 3 MV/cm for a SiC NMOS device will limit the maximum gate bias to only +15 V for the typical 50-nm gate dielectric thickness at room temperature. At higher temperatures, the electric field in the dielectric (and hence the gate bias) must be made even smaller in order for the SiC MOS reliability to approach that of a Si MOS transistor. Since the valence band offset of 3.05 eV is larger than the conduction band offset of 2.7 eV, PMOSFET reliability may be higher than NMOSFET reliability in the on-state of operation. Ironically, the wider bandgap of SiC seems like a liability rather than an asset for high-temperature operation because its band structure occupies a larger portion of the SiO_2 band structure.

From this discussion, it seems that the gate tunneling current of a conventional SiC NMOS device is higher than an Si NMOS devices at similar gate electric fields and temperatures. However, this conclusion is drawn from the worst-case scenario of assuming the barrier height for the purposes of FN tunneling is equal to the conduction band offset of 4H-SiC and SiO_2; i.e., the case of strong inversion. A significant gain in the barrier height may be achieved if the Fermi level in SiC is below the conduction band; i.e., an enhancement-mode MOSFET (with p-type SiC) under weak inversion condition [44]. The gate bias range when the MOSFET is under weak inversion conditions is determined by the doping of the p-type base region. At the onset of weak inversion, the barrier height (Φ_F) may be as much as 4.3 eV (1.6 eV + 2.7 eV, Φ_C), as can see seen from Figure 7. A barrier height of 4.3 eV will allow a higher temperature operation of 4H-SiC-based MOSFETs as compared to Si-based MOSFETs (with a maximum barrier height of 3.75 eV), for an identical on-state electric field in the dielectric. This assumes that channel mobilities for Si and 4H-SiC MOSFETs are similar for an identical electric field in the dielectric. However, despite more than a decade of research, relatively modest success has been achieved in the

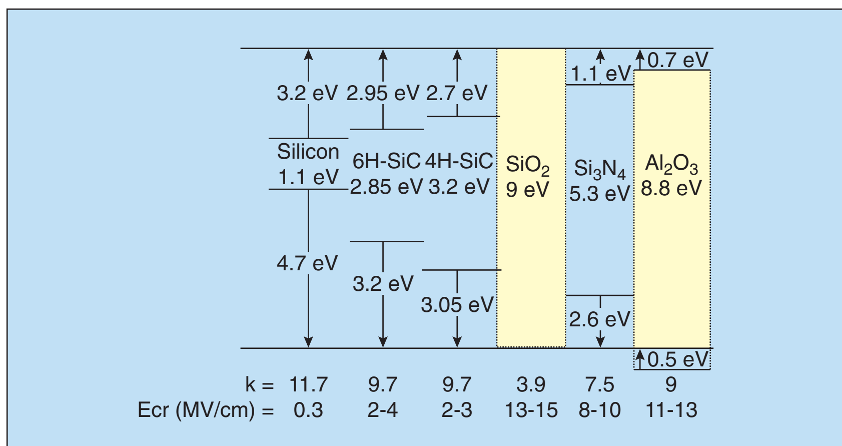

FIGURE 6 — Dielectric constants and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offsets are also shown with respect to SiO_2.

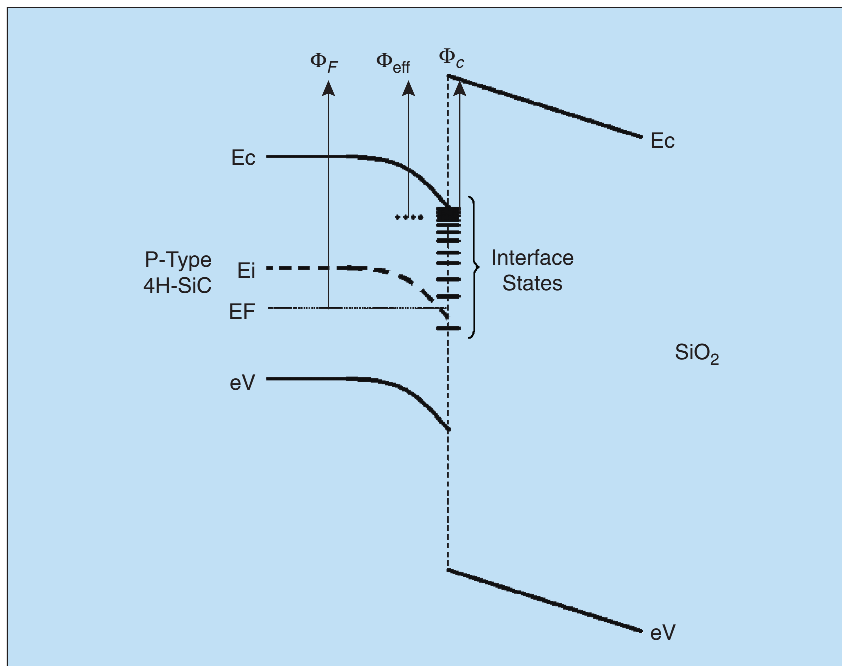

FIGURE 7 — SiC MOSFET under weak inversion case. The relevant barrier heights for FN tunneling in SiC-SiO_2 interface: Φ_C is the conduction band offset, Φ_F is the theoretical FN barrier height, and Φ_{eff} is the effective barrier height due to the presence of interface states at the SiC–SiO_2 interface.

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realization of high channel mobilities [49] for enhancement-mode NMOSFETs. Because of the low channel mobility observed in most 4H-SiC-based MOS devices, a higher gate bias (and electric field) may be required in order to realize a low channel resistance in a SiC power MOSFET. This represents a challenge for achieving a high reliability in SiC-based MOS devices at all temperatures. Hence, there exists an on-state performance/gate dielectric reliability tradeoff determined by the experimentally obtained channel mobility.

SiC-Dielectric Interface State Density

The performance/reliability tradeoff is severely influenced by traps and carrier energy states at the SiC-dielectric interface. The origin of these traps is linked to the imperfect nature of 4H-SiC/dielectric interfaces due to the presence of carbon clusters [50] and/or dangling Si- and C-bonds. A significant number of electrons that are expected to provide the low on-resistance of the inversion layer get trapped in these energy states and scatter mobile electrons, further increasing the resistance in the channel region. Experimental data by Ouisse [51] show that the low channel mobility in 4H-SiC is directly linked to extraordinarily high interface state densities in the SiO_2/SiC junctions. In the energy band diagram, the interface traps that influence channel mobility are located between the Fermi level and the conduction band of the SiC polytype used to make the MOSFET, as shown in Figure 7. Experimental data by Schorner [52] have shown that the density of these interface states in SiC exponentially increase beyond a level of 2.4 eV above the valence band of all SiC polytypes. In this study, the anomalously low electron inversion mobility in 4H-SiC MOSFETs (as compared to 3C, 6H, and 15R SiC) was attributed to the largest bandgap of 4H-SiC among the commonly studied SiC polytypes.

The location and density of interface states within the bandgap influences not only channel mobility but also the FN tunneling currents at the SiC-dielectric interface. The existence of a significant density of electrons at the interface states causes them to act as the primary source of FN tunneling current into the dielectric, rather than the position of the Fermi level [32]. Rather than a well-defined barrier height determined by the difference between the Fermi level and conduction band, an "effective" barrier height (Φ_{eff}) is typically observed in most cases, which is determined by the density and location of the interface states [32] in the energy gap. Since most of the interface states are located close to the conduction band edge, Φ_{eff} is close to the conduction band offset of the SiC-SiO_2 interface. FN tunneling current data on n-type SiC by Li et al. [53] shows that the "effective" barrier height is even lower than the 2.7-eV conduction band offset difference at room temperature, and it decreases to only 2.38 eV as the operating temperature is increased to 300 °C. Similarly, a lower FN tunneling barrier height was experimentally observed in 4H-SiC PMOSFETs by Chanana et al. [54], indicating the strong influence of interface states on FN tunneling current rather than the position of the Fermi level.

The low inversion layer mobility in power NMOSFETs may be acceptable for higher voltage (>2 kV) MOSFETs since a lower proportion of the resistance is contributed by the channel. However, if the MOS interface state density in these devices is high, their viability will be determined primarily by FN tunneling. The electric field in the dielectric must be kept correspondingly lower to limit FN tunneling current. The reduction in interface state densities in MOS structures will play a critical role in the on-state and high-temperature performance, as well as reliability of power MOSFETs in 4H-SiC.

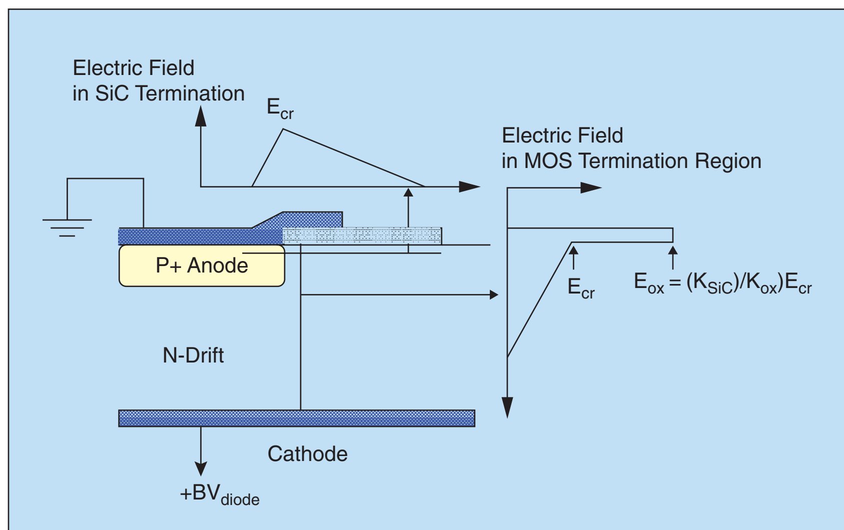

FIGURE 8 — Unterminated edge of a SiC PiN junction with a metal-oxide SiC stack beyond the PN junction. The electric fields in the SiC and the oxide-semiconductor interface are also shown.

MOS in Reverse Bias

In addition to reliability challenges faced by 4H-SiC MOS devices in the on-state, they must be carefully designed to ensure good reliability in the reverse-bias state. Consider an unterminated edge of a PiN diode with a lateral PiN region supporting the full blocking voltage, and a metal-oxide-SiC stack adjoining the PN junction, as shown in Figure 8. For this diode to support the full voltage capability of SiC, the peak electric field at the PN junction is close to the critical electric field of SiC, which is approximately 2.5 MV/cm. According to Gauss' Law, the electric field in the oxide is the inverse ratio of the dielectric constants, which are 9.7 and 3.9 for SiC and SiO_2, respectively. This implies that the electric field in the oxide is 6.2 MV/cm! Termination regions and other active regions in the devices must be designed carefully to prevent a high electric field at the SiC–SiO_2 interface.

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Note that for reverse-biased MOS, the bands bend in the opposite direction of that shown in Figure 7, and the relevant barrier height for FN tunneling corresponds to the valence band offset, rather than conduction band offset. In contrast to the forward-biased MOS case, the electric field in the dielectric is determined by its dielectric constant and interface electric field, rather than the thickness of the dielectric. The electric field in the oxide is not excessive in Si-based high-voltage devices because the critical electric field of Si is about an order of magnitude lower than SiC. The high critical electric field strength of SiC can only be utilized to obtain high-voltage SiC devices with SiO_2, which has the highest electric field strength of the commonly studied dielectrics, unless specific designs are adopted to alleviate the electric field in alternative dielectrics.

The issue of high electric fields in the dielectric is even more severe for power MOSFETs in SiC because it is generally more difficult to shield gate dielectrics from high electric fields. The three dominant families of Si and SiC power MOSFETs are: double (implanted) (D)MOSFETs, trench-gate or UMOSFETs, (U representing the shape of the gate) and lateral MOSFETs. For lateral MOSFETs, the oxide breakdown location is similar to that shown in Figure 8. For such MOSFETs [55], a high electric field exists at the p-base/drift region junction, resulting in a high electric field in the dielectric. In case of trench-gate MOSFETs or UMOSFETs [56], an extremely high electric field exists in the oxide at the trench bottom [57], adjacent to the voltage blocking p-base/n drift junction, as shown in Figure 9(a). The electric field concentration at the trench corners and the bottom is even more severe than the lateral case because the trench bottom must extend below the voltage blocking PN junction. A smaller pitch worsens rather than alleviates this problem because it will expose an even larger area of the trench bottom oxide to high electric field. The electric field at the trench bottom may be lowered to some extent by placing deep p-type extensions below the p-base region [58], in a principle similar to a junction barrier Schottky (JBS) diode.

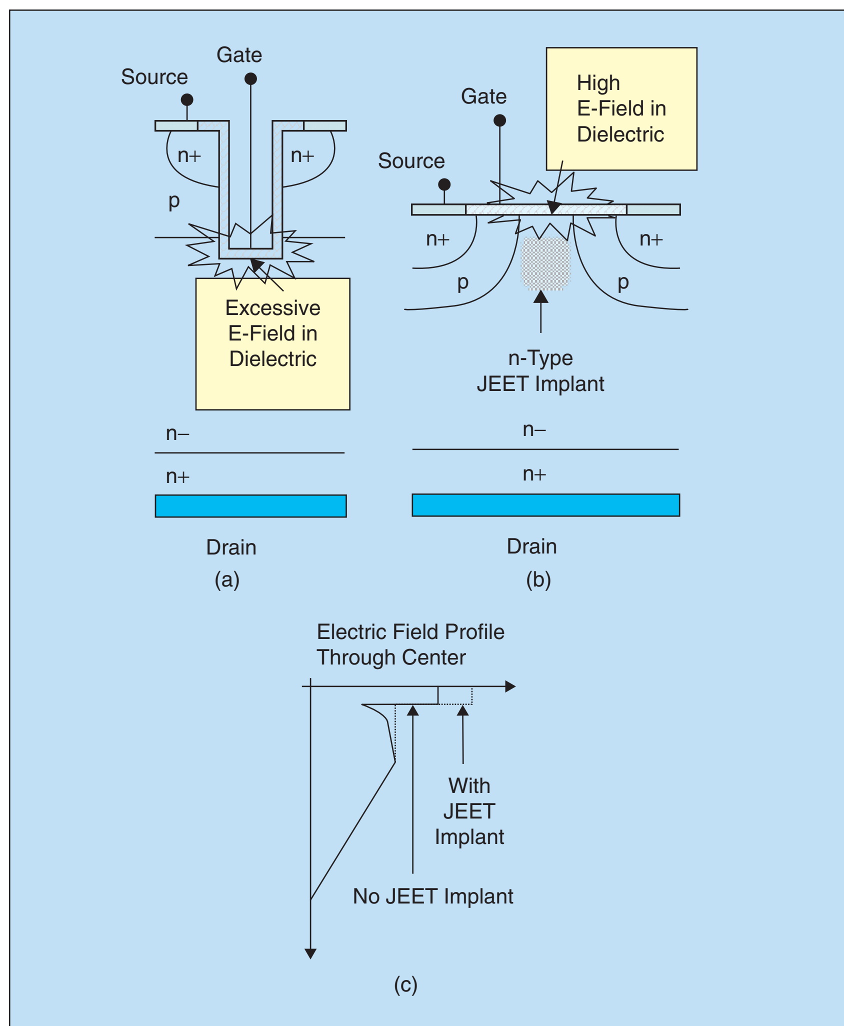

FIGURE 9 – High electric field location for (a) UMOSFETs and (b) DMOSFET power MOS structures. Electric field profile for a DMOSFET for the case with and without the JFET region implantation shown in (c).

The most promising structure for SiC power MOSFETs may be the DMOSFET structure, shown in Figure 9(b), from the standpoint of controlling the electric field in the gate oxide. The electric field at the SiC–SiO_2 interface is lowered by the electric field pinch-off effect from the adjacent p-base regions. This leads to an acceptably low electric field in the gate oxide shown through simulations in [59]. However, this pinch-off increases the resistance of the DMOSFET by introducing a "JFET" region between adjacent p-base regions. The tradeoff between the on-state resistance of the DMOSFET and the extent of reduction of the electric field at the SiC–SiO_2 interface is determined by the spacing of the adjacent p-base region, as discussed in detail in [59]. During the evolution of Si DMOSFETs, the reduction in cell pitch resulted in a very high JFET region resistance. Hence, it was necessary to increase the n-type concentration of the JFET region through, for example, n-type ion implantation. For very-high-voltage SiC DMOSFETs (>2 kV), the lower doping of the n-drift region will cause the JFET pinch-off to be severe, resulting in a high "JFET" region resistance. However, an n-type "JFET" implant in SiC DMOSFETs increases the electric field in the oxide to a higher level, as shown in Figure 9(c). This tradeoff is less critical for Si DMOSFETs because the electric field in the gate oxide for those devices is <1 MV/cm due to a lower critical electric field of Si.

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Conclusions

Despite the remarkable results demonstrated by many groups around the world in exploiting the superior properties of SiC for high-power and high-temperature devices, there are reliability issues faced by SiC as a material of choice for commercial power devices. Although some of these issues reflect the relative immaturity of this technology requiring years of development, some may be fundamental to this material.

Material defects in present-day SiC are the cause of many technological challenges faced by SiC devices. Wafer-level defects include micropipes, closed-core screw dislocations, basal plane dislocations, and low-angle grain boundaries. In the active device regions (epitaxial layers), some of these defects may be annealed if good epitaxial techniques are employed, but others result in a) reduced critical electric field in devices, b) higher leakage currents during reverse-bias operation, and c) degradation in the on-state performance of bipolar devices. Although many of these defects affect the reverse characteristics of high-voltage SiC devices, long-term operation of many devices has revealed that optimally processed devices do not suffer from reliability issues. This has allowed for the commercialization of the power SiC Schottky diode. Although the avalanche energy of SiC power devices is experimentally determined to be 3–10X higher than conventional Si power devices, material defects have been shown to cause filaments that concentrate the plasma of the avalanche current. Detailed experiments conducted recently on bipolar SiC devices have shown that the on-state voltage drop in such devices increases with time when they are kept in the forward-biased mode for an appreciable length of time. Optical observation of PN diodes undergoing V_F degradation shows a simultaneous formation of mobile and propagating crystal stacking faults that are responsible for a reduction in the diode conduction area.

The performance/reliability tradeoff for SiC MOS-based devices like power MOSFETs and IGBTs is more severe than Si power MOSFETs because of the substantially lower MOS channel mobilities, smaller barrier height to tunneling, and higher experimentally obtained interface state densities. An approach investigated in this article is the use of alternative dielectrics with higher dielectric constants, which may reduce the electric field in SiC MOS devices. However, many of these materials suffer from correspondingly lower breakdown field strength. High breakdown electric field strength of SiC also affects the choice of passivating dielectrics used in the edge termination and active regions of power devices.

Since the electric fields in dielectrics scale inversely with their dielectric constants, SiO_2 sees a 10X higher electric field during reverse-bias operation of these devices as compared to Si devices. This problem is further exacerbated in trench-gate MOSFETs because of field crowding at trench corners. This is another motivation for exploring high dielectric constant/high dielectric strength materials for SiC power devices. The higher bandgap of SiC has often been cited as a reason for pursuing high-temperature power devices because of their correspondingly lower leakage currents. However, the reverse-leakage currents in Schottky-based devices are dominated by the Schottky barrier height of these materials. Since the barrier height of commonly used Schottky metals for SiC devices is in the 0.7–1.2-eV range, the temperature performance of these devices will be similar to Si PN junction-based devices. This problem gets very severe in power MESFETs because the gate regions routinely see a much higher local temperature as compared to the device ambient temperatures.

Biographies

Ranbir Singh received the B. Tech. degree from the Indian Institute of Technology, New Delhi, India, in 1990 and the M.S. and Ph.D. degrees from North Carolina State University, all in electrical engineering. He was with Cree Inc. in Durham, North Carolina, from 1995 to 2003. Then he was with the National Institute of Standards and Technology, Gaithersburg, Maryland. Thereafter, he founded GeneSiC Semiconductor Inc. He has coauthored over 90 journal papers and conference proceedings and is an inventor on 20 issued U.S. patents. He was on the technical committee of the International Symposium on Power Semiconductor Devices and ICs (ISPSD) from 2002 to 2004. In 2003 and 2004 he received the IEEJ Technical Development Award for the development of ultra-high-voltage SiC devices. He is the author of the book *Cryogenic Operation of Silicon Power Devices* (Kluwer, 1998).

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