15 kV SiC PiN diodes achieve 95% of avalanche limit and stable long-term operation

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Abstract— **This paper reports on ultra-high voltage, >15 kV SiC PiN rectifiers exhibiting >95% of the avalanche rating and 115 V/µm. This is one of a few reports on > 15 kV blocking voltages measured on any single semiconductor device, and the highest percentage of the avalanche limit ever reported on devices fabricated on > 100 µm thick SiC epilayers. Excellent stability of on-state voltage drop (V_F) is displayed by 5.76 mm^2 and large-area, 41 mm^2 PiN rectifiers, when continually biased at high current densities for several days. The impact of carrier lifetime on the device performance for SiC bipolar devices with ultra-thick (≥100 µm) base layers is investigated by comparing I-V-T characteristics of SiC PiN rectifiers fabricated on 100 µm and 130 µm thick epilayers.**

I. INTRODUCTION

At 10 kV – 20 kV voltage ratings, 4H-SiC PiN rectifiers offer the best trade-off between on-state voltage drop, switching losses and high-temperature performance as compared to Si PiN or SiC Schottky/JBS rectifiers. These ultra-high voltage SiC PiN rectifiers are being developed as companion free-wheeling diodes for GeneSiC's future product portfolio of 10-15 kV SiC transistors. This paper reports on detailed results from experimental on-state, blocking and long-term reliability characterization performed on SiC PiN rectifiers fabricated on 130 µm thick n- epilayers.

II. EXPERIMENTAL

SiC PiN rectifiers with 2.4 mm x 2.4 mm chip size (active area = 5.76 mm^2) and 6.4 mm x 6.4 mm chip size (active area = 41 mm^2) were fabricated on 130 µm thick, 6-7 x 10^{14} cm^{-3} doped n- 4H-SiC epilayers. The p+ emitter layers were 1.5 µm thick and doped to 1 x 10^{19} cm^{-3}. Optimized edge termination for the PiN rectifiers was provided by a combination of GeneSiC-pioneered beveled mesa etching and p-type ion-implantation followed by high-temperature annealing for implant activation. Ohmic contacts to the p+ Anode and n+ Cathode layers was formed by Al-based and Ni- based metallization. Thick Al overlayers were deposited on the top and a solderable Au-based metallization was provided on the bottom for die-attaching to Cu baseplates. After on-wafer testing, selected die were assembled in custom- designed packages for detailed high-current, switching and long-term measurements.

III. BLOCKING VOLTAGE MEASUREMENTS

The onset of sharp avalanche breakdown at 15 kV (Figure 1) is observed on several PiN rectifiers, with extremely low-leakage currents preceding the breakdown voltage. The achievement of 15 kV blocking voltages corresponds to 115 V/µm and 95% of the avalanche breakdown limit for the 130 µm thick n- epilayer, calculated by direct integration of the 4H-SiC impact ionization co-efficients [1].

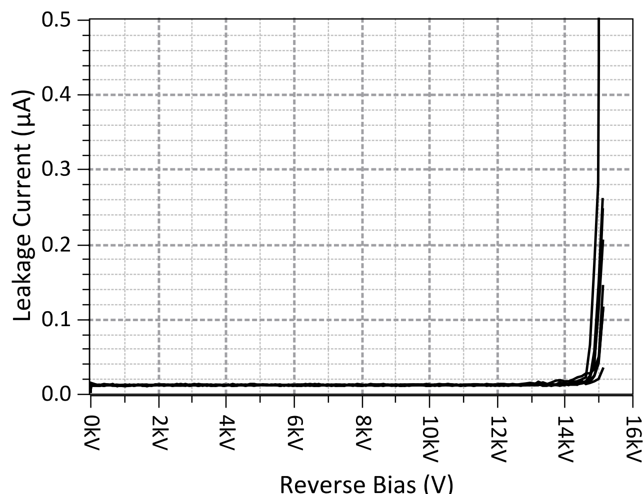

Figure 1. 15 kV blocking voltages measured on several PiN diodes fabricated on 130 µm thick, 6x10^{14} cm^{-3} doped n- SiC epilayers, which corresponds to >95% of the avalanche breakdown limit.

IV. ON-STATE CHARACTERISTICS

An on-state voltage drop (V_F) of 6 V and differential on-resistance of 15.5 mΩ-cm^2 are measured on the 5.76 mm^2 rectifiers (Figure 2a) at 100 A/cm^2 and 25 °C, which reduce to 4 V and 8 mΩ-cm^2, respectively, at 225 °C. Likewise, the 41 mm^2 rectifiers also exhibit a negative temperature co-efficient of V_F (at 10 A) and $r_{on,sp}$ (Figure 2b) – 4.1 V and 25.5 mΩ-cm^2 at 25 °C; 3.3 V and 9.9 mΩ-cm^2 at 175 °C. The negative

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temperature co-efficient of V_F measured on both the 5.76 mm^2 and 41 mm^2 PiN rectifiers is due to increasing high-level carrier lifetime (t_{HL}) and the reduction of the built-in voltage at higher temperatures. The larger on-resistance recorded on the 41 mm^2 rectifiers could be due to the less-effective vertical current spreading, and higher parasitic top metal spreading resistance.

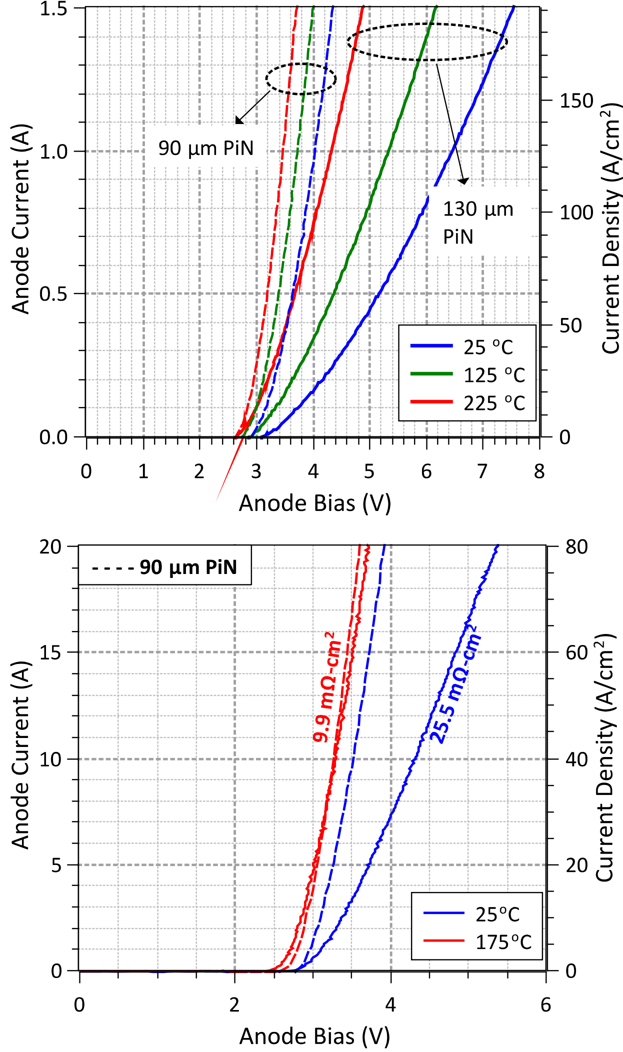

Figure 2. Forward bias I-V-T characteristics measured on (Top,a): 5.76 mm^2 PiN rectifiers and (Bottom,b): 41 mm^2 PiN rectifiers, both fabricated on 130 µm thick/6e10^{14} cm^{-3} doped n- epilayers. For comparison, the 25°C and 175°C forward bias characteristics previously reported on 41 mm^2 rectifiers fabricated on 85 µm epilayers are also shown in (b).

The temperature variation of $r_{on,sp}$ for these 130 µm PiN rectifiers are compared in Fig. 2 with the results reported earlier [2] on PiN rectifiers fabricated on 90 µm thick SiC epilayers. Significantly lower on-resistance and a much softer temperature dependence of $r_{on,sp}$ is observed in Fig. 3 for the PiN rectifiers fabricated on 90 µm thick SiC epilayers, as compared to the 15 kV rectifiers reported in this article. The on-resistance of a PiN rectifier is a function of the extent of conductivity modulation of the n- drift layer. Since very similar values (≈ 5 µs) of carrier lifetime were recorded on both the 90 µm and 130 µm thick SiC epiwafers by microwave photoconductive decay (µ-PCD), this suggests that the carrier lifetimes in the 130 µm thick SiC epilayers although high by 4H-SiC standards, are not sufficient for complete conductivity modulation of the entire thickness of the drift region. A first order estimate for the minimum carrier lifetime (t_{HL}) for complete conductivity modulation of an n-type 4H-SiC base layer can be expressed as:

$$t_{HL} = d^2/4D_a \qquad (1)$$

where d is the base layer thickness and D_a is the ambipolar diffusion co-efficient, which can be easily derived using the electron and hole mobilities for 4H-SiC for the particular doping concentration of the n- epilayer. Plugging in electron and hole mobilities [3] of 800 cm^2/Vs and 80 cm^2/Vs to calculate D_a in (1), the minimum required t_{HL} can be calculated as 5 µs for a 90 µm thick n- epilayer, while it increases to 11.5 µs for a 130 µm thick epilayer. OCVD measurements on PiN rectifiers fabricated on 90 µm thick epilayers [2] showed that t_{HL} increased from 4.5 µs at 25°C to 14 µs at 225°C, which can explain the drastic decrease in the $r_{on,sp}$ measured on the 130 µm PiN rectifiers at elevated temperatures. These results suggest that for optimum conductivity modulation of the ultra-thick (> 100 µm) SiC epilayers that are necessary for > 10 kV device fabrication, epi-growth or processing strategies for increasing the (room-temperature) t_{HL} above 10 µs need to be pursued. The carrier lifetime enhancement by the deep level reduction (DLR) process proposed in [4] is one alternative to increase the carrier lifetime during device processing. These approaches will be the subject of future investigations at GeneSiC.

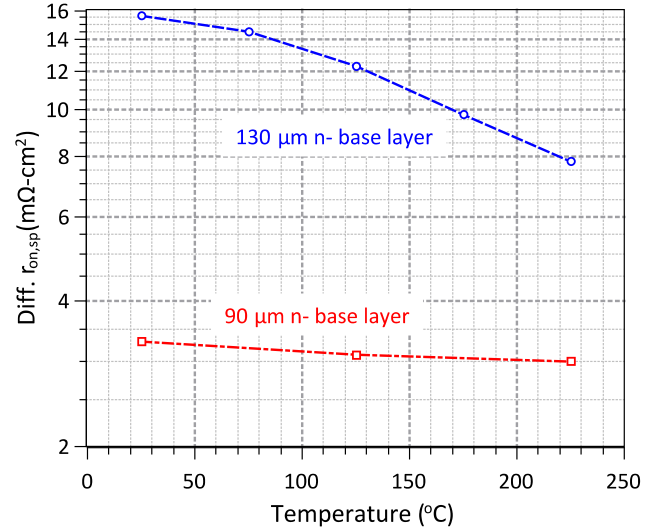

Figure 3. Temperature dependence of differential specific on-resistance in the range of 0.7-0.8 A, for 5.76 mm^2 PiN rectifiers fabricated on 90 µm and 130 µm thick n- epilayers

V. FORWARD BIAS DRIFT STABILITY

One of the remaining bottlenecks for the commercialization of SiC bipolar devices is the basal plane dislocation (BPD) related drift of the on-state voltage drop, when biased continuously under forward bias conditions. We have previously reported [2] drift-free operation of SiC PiN rectifiers fabricated on 90 µm thick epilayers. In this work,

representative 5.76 mm^2 and 41 mm^2 PiN rectifiers after packaging in special test coupons were subjected to continuous operation at forward bias current densities of 100 A/cm^2 (0.8 A) and 40 A/cm^2 (10 A) for 90 hours and 55 hours, respectively, at a controlled base plate temperature of 25°C. As shown in Fig. 4, after an initial stabilization of 5-10 hours, the VF of these PiN rectifiers displays excellent stability within 10 mV for the remainder of the duration of the test. The exact reasons for the contrasting trends shown by the 5.76 mm^2 and 41 mm^2 rectifiers during the initial stabilization period is unknown at this time. We did not observe any such stabilization period during our previous study on 90 µm PiN rectifiers.

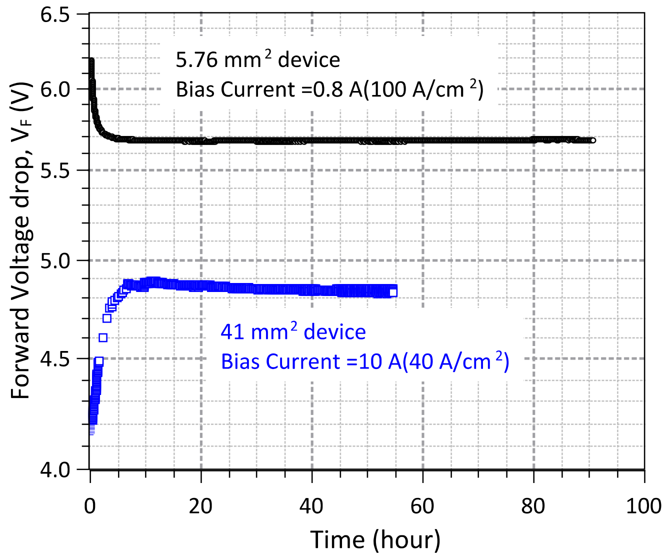

Figure 4. Evolution of on-state voltage drop (V_F) for the 5.76 mm^2 and 41 mm^2, 15 kV SiC PiN rectifiers under DC current stress of 0.8 A (100 A/cm^2) and 10 A (40 A/cm^2), respectively. After an initial period of 5-10 hours, the V_F exhibits excellent stability for the remainder of the test duration.

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