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Stability of Electrical Characteristics of SiC "Super" Junction Transistors under Long-Term DC and Pulsed Operation at various Temperatures

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ABSTRACT

The reliability of the electrical characteristics of SiC "Super" Junction Transistors (SJTs) is investigated under long-term avalanche-mode, DC and pulsed-current operation. There is absolutely no change in the blocking I-V characteristics after a 934 hour repetitive avalanche stress test. Long-term operation of the Gate-Source diode (open-Drain mode) alone does not result in any degradation of the on-state voltage drop (V_F) or current gain (β). Long-term operation in common-Source mode results in negligible V_F or β degradation, if the base-plate is maintained at 25 °C. A greater degradation of β results with increasing base-plate temperature. The same total electrical charge, if passed through the SJT as a pulsed current instead of a DC current results in a smaller β reduction. It is also shown that this β degradation can be reversed by annealing at ≥ 200 °C, suggesting the possibility of degradation-free operation of SiC SJTs, when operating in pulsed current mode at ≥ 200 °C temperatures.

INTRODUCTION

Silicon Carbide (SiC) "Super" Junction Transistors (SJTs) are high current gain, majority-carrier transport, SiC NPN Bipolar Junction Transistors (BJTs) developed by GeneSiC in 1200 V -10 kV ratings. 1200 V/5 A rated SiC SJTs with current gains (β) as high as 88, and ultra-fast switching times of < 15 ns were recently reported [1]. In this study, a comprehensive evaluation of the stability of the SJT electrical characteristics after long-term operation is presented. The stability of the leakage currents in blocking mode after single-pulse and repetitive forced-avalanche mode operation of the SiC SJT are also investigated.

There are several publications [2,3,4,5] that discuss the stability of the current gain (β) and on-state voltage drop (V_F) of SiC BJTs, when the devices are subjected to long-term open-Collector or common-Source operation. These reports contain conflicting results ranging from near-perfect β and V_F stability to significant gain compression. Therefore, a key focus of this work is an attempt to resolve these conflicting reports by examining the stability of β and V_F of SiC SJTs under various long-term operating conditions including DC or pulsed-current regimes, and at actively controlled case temperatures ranging from 25 °C to 125 °C.

EXPERIMENTAL

Several 1200 V/5 A-rated SiC SJTs fabricated and packaged in test coupons at GeneSiC were used for performing the reliability characterization for this study. For the long-term stability measurements of the SJT on-state characteristics, a custom-designed test bench consisting of an active temperature controlled hotplate was used to achieve a constant base-plate temperature during the long-term operation of the devices. The SJTs were triggered by an off-the-shelf Si

IGBT Gate driver. A 100 nF dynamic capacitor connected across a 22 Ω Gate resistor provided high transient currents for fast sub-20 ns SJT switching (see ref [1] for more details on the Gate drive scheme). For the forced-avalanche mode tests, an unclamped inductive load test setup [1] was used.

RESULTS AND DISCUSSION

Avalanche Ruggedness

Previously [1], a single-pulse avalanche energy rating of 20.4 mJ by unclamped inductive switching of a 1200 V/5 A SiC SJT was reported. In this work, the stability of the blocking I-V characteristics after both single-pulse and repetitive avalanche regime operation is investigated. A 1200 V/5 A SiC SJT was subjected to five, 3.9 mJ pulses in the avalanche regime (see waveform in Figure 1(a)), and the blocking I-V characteristics were measured after each test. There was no change in the blocking characteristics of the SJT before and after the application of the avalanche mode pulses.

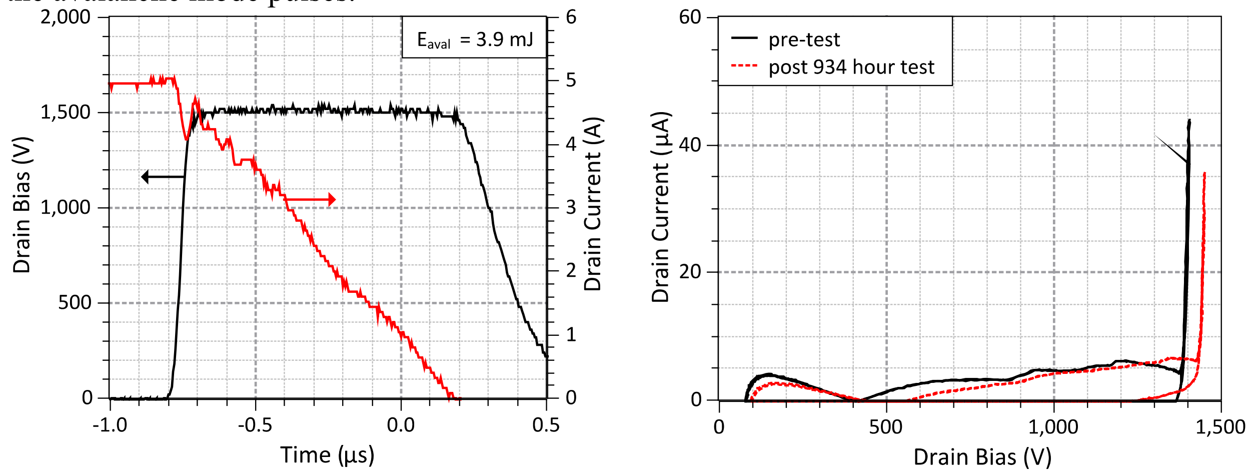

Figure 1 (a, Left): Example waveform of a 1200 V/5 A SJT dissipating 3.9 mJ under avalanche mode conditions and (b, Right): Examination of the Drain-Source blocking characteristics of the SJT before and after a repetitive avalanche-stress applied to the device for 934 hours.

In a separate experiment, another device was subjected to repetitive 2.3 mJ avalanche mode pulses with a frequency of 14.3 kHz and a duty cycle of 30%. This test was run for 934 hours. The blocking I-V characteristics measured before and after this long-duration test (Figure 1(b)) actually indicates a slight improvement of the breakdown voltage from 1400 V to 1450 V, after 934 hours of operation under repetitive avalanche pulses. These results indicate that the SiC SJTs reported in this study offer stable operation, even after long-term avalanche-mode operation. This clearly distinguishes the SJTs from Si BJTs, which undergo destructive failure, when exposed to avalanche-mode conditions.

Stability of the Current Gain and On-State Voltage Drop after long-term operation

In this study, a comprehensive set of experiments were performed to better understand the long-term stability of the on-state characteristics of the SiC SJTs, specifically the current gain (β) and V_F. A series of long-term operation tests with varying base-plate temperature, on-pulse duration (duty-cycle) and switching frequency were performed. For all the tests, the exact same Gate driving scheme used for the obtaining the switching waveforms was employed. The current gain (β) was always calculated at a Drain Current of 5 A.

Influence of base-plate temperature: A set of long-term DC operation tests with a constant drain current of 5 A and a Gate current of 250 mA were performed on several 1200 V SJTs, at base-plate temperatures ranging from 25 °C to 125 °C. All devices selected for these experiments had a starting β in the range of 68-72. The devices were continuously biased for 5.8 hours and the on-state characteristics were periodically obtained by interrupting the tests, from which the β and V_F were extracted. The evolution of β versus test duration is shown in Figure 2, where it can be clearly seen that a higher base-plate temperature results in a greater reduction of β. This indicates that the carrier trapping mechanism responsible for current gain reduction is more efficient at higher junction temperatures.

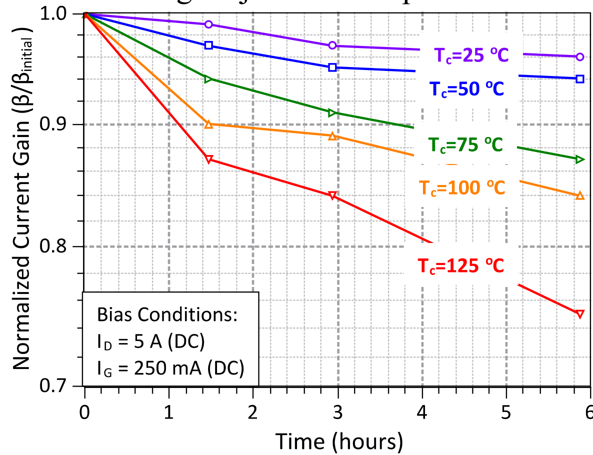

Figure 2 (a, Top-Left): Variation of the normalized current gain (β) at a Drain current of 5 A, after long-term DC operation at various base-plate temperatures; (b, Top-Right): SJT Output Characteristics before and after the long-term DC bias at T_C = 25 °C; (c, Bottom-Left): SJT Output Characteristics before and after the long-term DC bias at T_C = 125 °C.

From Figure 2, a negligible β reduction (from 68.5 to 66) after 5.8 hours of DC operation is obtained, when the base-plate temperature is maintained at 25 °C. However, a significant β reduction from 69.4 to 52 is observed in 5.8 hours, when the base-plate temperature was increased to 125 °C. A comparison of the SJT output characteristics before and after the 5.8 hour DC bias test at a base-plate temperature of 25 °C revealed no change in the device on-resistance after the test. On the other hand, the 5.8 hour DC test at a base-plate temperature of 125 °C resulted in a finite increase of the V_F by 300 mV at a Drain current of 5 A. However, no quasi-saturation region was detected in the output characteristics, as observed in [3]

DC versus pulsed current long-term operation*:* It was reported in [6] that the same charge passing through a SiC PiN diode as a DC or pulsed current causes fundamentally different V_F shifts, with the pulsed current causing smaller V_F shifts than the DC current. In this work, selected SiC SJTs were subjected to long-duration, 5 A DC or pulsed currents, applied with a pulse width of 30 µs, and at a switching frequency of 14.3 kHz and at a case temperature of 125 °C. The DC and pulsed-mode operation are compared by plotting the evolution of β versus the total charge impressed upon the device as the ordinate axis in Figure 3(a). The β reduced to 82% of its pre-test value after a 15.9 hour pulsed-current test, while the 5.9 hour DC-current test reduced the β to 75% of its pre-test value, even though the same total electrical charge (106 kC) was impressed on the device during the two tests. This result is consistent with the smaller V_F shift observed under pulse-currents versus DC currents [6] for SiC PiN diodes.

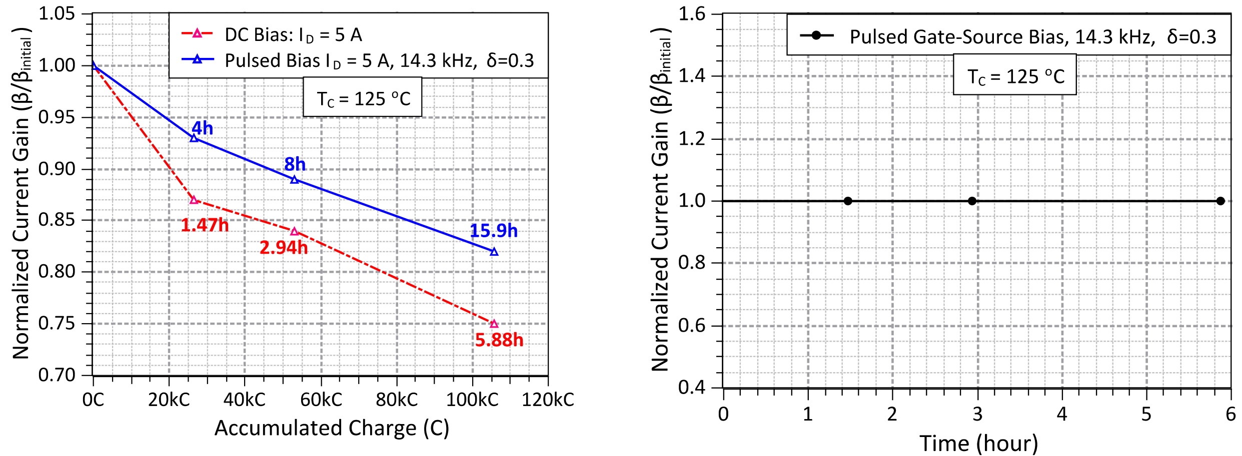

Figure 3 (a, Left): Variation of normalized SJT current gain (β) after passing 5 A of Drain current either as a DC current or as a pulsed current; (b, Right): Absolutely no variation of SJT current gain is observed after a 5.8 hour open-Drain pulsed current test.

Long-term Open-Drain operation: In this work, long-term (15.8 hour) pulsed testing of the Gate-Source diode of a SiC SJT (or Open-Drain operation) was conducted at a duty-cycle of 30% and at a switching frequency of 14.3 kHz. The same Gate drive used for the previously described tests was used, i.e. an initial peak Gate current of 4.5 A for 100 ns followed by a plateau of 250 mA, and a peak reverse Gate current of -1 A. The base-plate temperature was maintained at 125 °C to enhance the gain degradation, if any. Figure 3(b) shows absolutely no reduction in the β after the 5.8 hour open-Drain long-term test. In contrast, the β decreased to 82% of its initial value, when a SJT was subjected to 5 A Drain current pulses in the common-Source mode for the same duration, with the same Gate drive, duty cycle, frequency and base-plate temperature (see Figure 2). This finding is in agreement with the results reported by Lindgren et al [7], who also showed zero change in the output characteristics of SiC BJTs after a 660 hour open-Collector stress by a Base current of 200 mA.

Factors responsible for Current Gain Reduction: From the results reported in Figures 2 and 3, it is clear that a greater current gain reduction over time is possible by (A) increasing the base-plate temperature and (B) operation in DC mode versus pulsed mode. According to this line of reasoning, the invariance of current gain observed after the open-Drain test may be due to a lower junction temperature in comparison with the common-Source test. The sub-threshold Gate-Source I-V characteristics, examined before and after the above-mentioned long-term operation tests by Gummel Plot measurements (not shown), showed a marked Gate current increase in the sub-threshold region, in agreement with the simulations performed by Buono et al [2].

However, there was no change in the OCVD measured high-level carrier lifetime (t_{HL}) in the base layer (not shown) before and after the long-term operation tests. Since the OCVD technique measures the carrier lifetime in the bulk of the base layer [8], this implies that carrier traps are generated at the Gate-Source junction periphery after the long-term operation, most likely at the interface of the surface passivation and the SiC surface. The higher junction temperatures resulting from operating the SJT at either a higher base-plate temperature or a higher duty cycle/lower frequency increases the capturing efficiency of these traps, which results in a greater current gain compression. The absence of a quasi-saturation region in the output characteristics after the long-term operation also suggest that the positive V_F shift observed after the long-term operation is associated with the reduced emitter injection efficiency of the Gate-

Source p-n junction, and is not due to the presence of basal plane dislocations in the lightly doped n- drift layer, as observed by Konstantinov et al [3].

Current Gain Recovery by Thermal Annealing

There are reports [9] indicating that the V_F shift caused by long-term operation of SiC bipolar devices can be recovered by thermal annealing in the range of 300-400 °C for several hours. The SJTs subjected to long-term operation at various base-plate temperatures in this work (see Figure 2(a)) were later subjected to various sequential annealing treatments at 200 °C, 240 °C and 300 °C, in a temperature controlled oven to investigate possible recovery of the current gain.

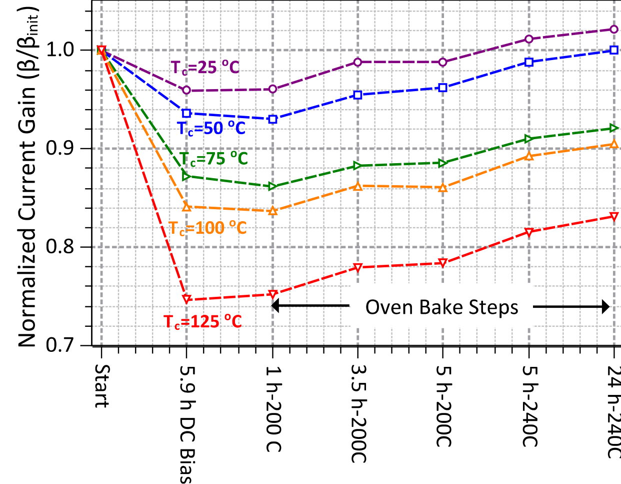

Figure 4: Current Gain Recovery of SiC SJTs subjected to long-term DC bias tests achieved by baking in a temperature controlled oven.

As shown in Figure 4, it can be seen that all previously degraded devices show a current gain recovery upon thermal annealing. Similar to current gain deterioration, the β recovery appears to be temperature dependent. There appears to be a maximum possible recovery of β at a given temperature. After 4.5 hours of annealing at 200 °C, a further 5 hour annealing at the same temperature did not further recover the current gain. However, the β recovers further after a subsequent 240 °C/5 hour annealing. It is observed from Figure that for a maximum annealing temperature of 300 °C, a full recovery of current gain is achieved for SJTs whose β was degraded up to 20%. Packaging limitations precluded annealing at temperatures higher than 300 °C. Interestingly, the β of mildly degraded devices are even higher than their corresponding pre-test value, after the thermal annealing.

In-situ recovery of current gain*:* The experimental results presented in this paper create an intriguing prospect for in-situ recovery of the current gain of SiC SJTs by operating them in the pulsed mode at high (≥ 200 °C) ambient temperatures. It is possible that any β degradation occurring during the on-pulse could be recovered during the off-pulse, provided the off-pulse is long enough for complete recovery. Long-term electrical stressing of SiC PiN diodes [10] and MPS diodes [9] at 242 °C and 200 °C, respectively resulted in a recovery rather than degradation of V_F. Further tests need to be performed to investigate long-term SJT operation under these high ambient temperature conditions.

CONCLUSIONS

A comprehensive evaluation of the reliability of the on-state and blocking voltage characteristics of SiC SJTs is presented in this paper. In stark contrast to Si BJTs, the SiC SJTs presented in this study are found to be operable under avalanche-mode conditions, with

absolutely no change to the blocking I-V characteristics, even after a 934 hour repetitive avalanche operation. The current gain and V_F are reasonably stable, when the device is operated at 5 A (146 A/cm^2) for several hours at a controlled base-plate temperature of 25 °C. Long-term DC operation at higher base-plate temperatures results in a greater reduction to the current gain and V_F. It was also found that the current gain reduction is significantly smaller, if the same charge is passed through the device as a pulsed current instead of a DC current. Operation of the Gate-Source diode alone did not result in any change to the output characteristics. Interestingly, the current gain degradation could be partially recovered by baking the devices in a temperature controlled oven at 200 °C - 240 °C. This raises the possibility of an in-situ recovery of any degradation of the current gain by operating the SJTs in pulsed mode at high (> 200 °C) ambient temperatures.

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