

G3R12MT12-CAL

1200 V 12 mΩ SiC MOSFET



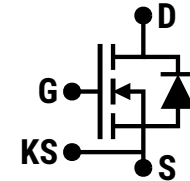
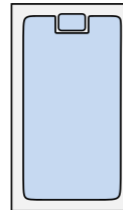
Silicon Carbide MOSFET
N-Channel Enhancement Mode

V_{DS}	=	1200 V
$R_{DS(ON)(Typ.)}$	=	12 mΩ
$I_D(T_C = 100^\circ C)$	=	136 A

Features

- G3R™ Technology with +15 V Gate Drive
- Softer $R_{DS(ON)}$ v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller $R_{G(INT)}$ and Lower Q_G
- Low Device Capacitances (C_{OSS} , C_{RSS})
- Superior Cost-Performance Index
- Robust Body Diode with Low V_F and Low Q_{RR}
- Industry-Leading UIL & Short-Circuit Robustness

Bare Chip



D = Drain
G = Gate
S = Source
KS = Kelvin Source



Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Better Power Density and System Efficiency
- Ease of Paralleling without Thermal Runaway
- Higher System Reliability

Applications

- EV Traction Inverters
- Industrial Motor Drives
- Solar Inverters
- Off-Board Chargers
- Solid State Circuit Breakers
- Switched Mode Power Supplies
- Pulsed Power

Absolute Maximum Ratings (At $T_C = 25^\circ C$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	$V_{GS} = 0 V, I_D = 100 \mu A$	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +20	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +15	V	
Continuous Forward Current	I_D	$T_C = 25^\circ C, V_{GS} = -5 / +15 V$	180	A	
		$T_C = 100^\circ C, V_{GS} = -5 / +15 V$	136		
		$T_C = 135^\circ C, V_{GS} = -5 / +15 V$	110		
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq 3 \mu s, D \leq 1\%, V_{GS} = 15 V, \text{Note 1}$	400	A	
Power Dissipation	P_D	$T_C = 25^\circ C$	820	W	Note 2
Non-Repetitive Avalanche Energy	E_{AS}	$L = 1.0 mH, I_{AS} = 50.0 A$	1204	mJ	
Operating and Storage Temperature	T_j, T_{stg}		-55 to 200	$^\circ C$	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

Electrical Characteristics (At $T_C = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	1200			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$		1		μA	
Gate Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$			-100		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50.0\text{ mA}$	1.8	2.70		V	Fig. 9
		$V_{DS} = V_{GS}, I_D = 50.0\text{ mA}, T_j = 200^\circ\text{C}$		2.00			
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 100\text{ A}$		48.0		S	Fig. 4
		$V_{DS} = 10\text{ V}, I_D = 100\text{ A}, T_j = 200^\circ\text{C}$		55.0			
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 100\text{ A}$		12	15	mΩ	Fig. 5-8
		$V_{GS} = 15\text{ V}, I_D = 100\text{ A}, T_j = 200^\circ\text{C}$		19			
Input Capacitance	C_{iss}			9334			
Output Capacitance	C_{oss}			283		pF	Fig. 11
Reverse Transfer Capacitance	C_{rss}			22.8			
C_{oss} Stored Energy	E_{oss}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		110		μJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			412		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			343		pF	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			515			
Gate-Source Charge	Q_{gs}	$V_{DS} = 800\text{ V}, V_{GS} = -5/+15\text{ V}$		80		nC	Fig. 10
Gate-Drain Charge	Q_{gd}	$I_D = 100\text{ A}$		112			
Total Gate Charge	Q_g	Per IEC607478-4		288			
Internal Gate Resistance	$R_{G(int)}$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		1.2		Ω	
Turn-On Switching Energy (Body Diode)	E_{on}	$T_j = 25^\circ\text{C}; V_{GS} = -5/+15\text{V}; R_{G(ext)} = 2\ \Omega, I_D = 100\text{ A}; V_{DD} = 800\text{ V}$		491		μJ	Fig. 18
Turn-Off Switching Energy (Body Diode)	E_{off}			239			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, V_{GS} = -5/+15\text{V}$ $R_{G(ext)} = 2\ \Omega, I_D = 100\text{ A}$		24		ns	Fig. 20
Rise Time	t_r			33			
Turn-Off Delay Time	$t_{d(off)}$		Timing relative to V_{DS} , Resistive load		22		
Fall Time	t_f			19			

*The chip technology was characterized up to 200 V/ns. The measured dV/dt was limited by measurement test setup and package.

Note 2: Assuming $R_{thJC(max)} = 0.21^\circ\text{C/W}$

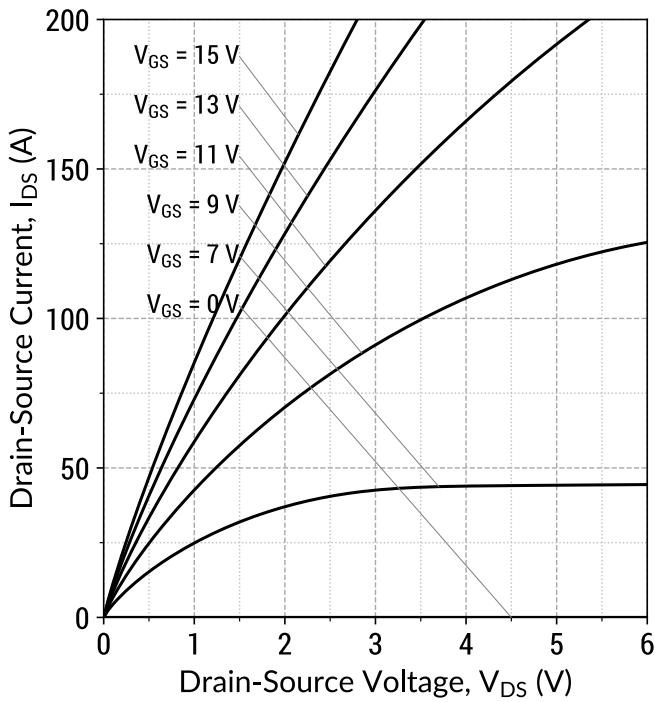
Note 3: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V.

$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{oss} while V_{DS} is rising from 0 to 800V.

Reverse Diode Characteristics

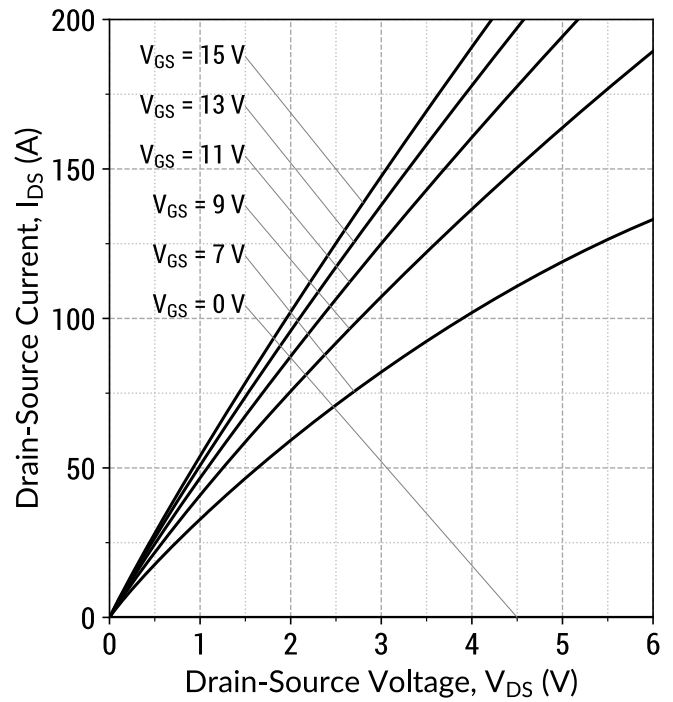
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}$ $V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, T_j = 200^\circ\text{C}$		4.7 4.2		V	Fig. 13-14
Continuous Diode Forward Current	I_S	$V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$	87			A	
Diode Pulse Current	$I_{S(pulse)}$	$V_{GS} = -5\text{ V}, \text{Note 1}$		348		A	
Reverse Recovery Time	t_{rr}			37		ns	
Reverse Recovery Charge	Q_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 100\text{ A}, V_R = 800\text{ V}$ $dif/dt = 2000\text{ A}/\mu\text{s}, T_j = 25^\circ\text{C}$		405		nC	
Peak Reverse Recovery Current	I_{rrm}			28		A	
Reverse Recovery Time	t_{rr}			61		ns	
Reverse Recovery Charge	Q_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 100\text{ A}, V_R = 800\text{ V}$ $dif/dt = 2000\text{ A}/\mu\text{s}, T_j = 200^\circ\text{C}$		1053		nC	
Peak Reverse Recovery Current	I_{rrm}			45		A	

Figure 1: Output Characteristics ($T_j = 25^\circ\text{C}$)



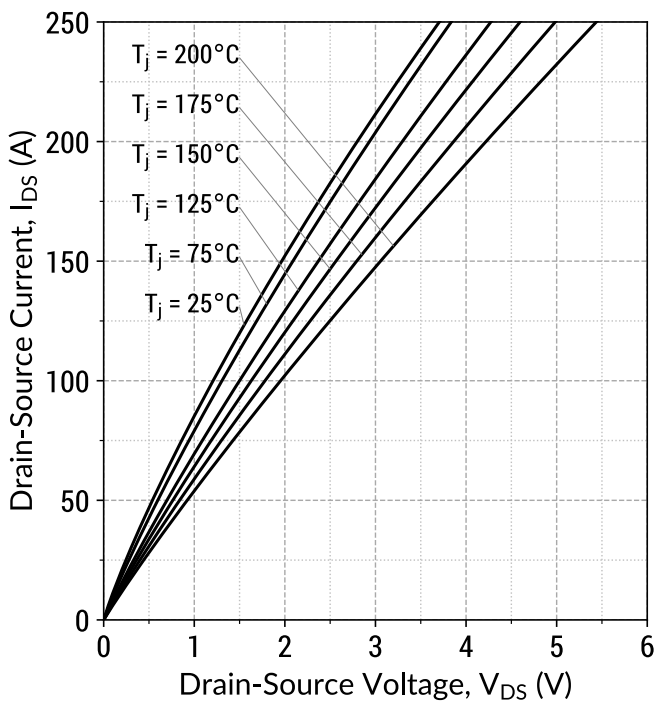
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 2: Output Characteristics ($T_j = 200^\circ\text{C}$)



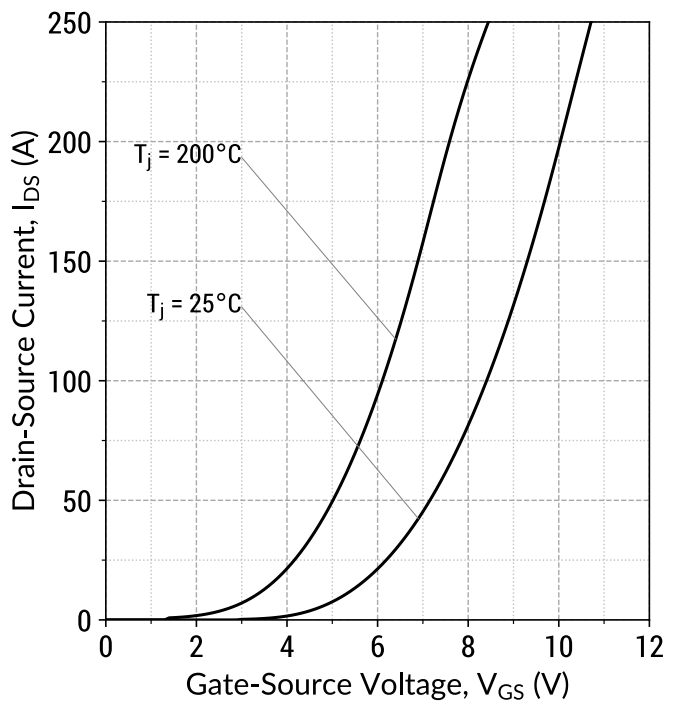
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 3: Output Characteristics ($V_{GS} = 15\text{ V}$)



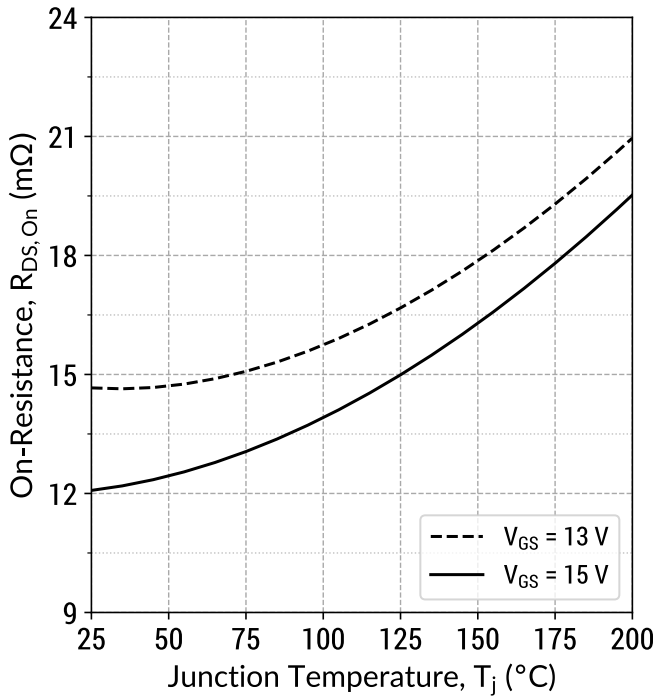
$$I_D = f(V_{DS}, T_j); t_P = 250 \mu\text{s}$$

Figure 4: Transfer Characteristics ($V_{DS} = 10\text{ V}$)



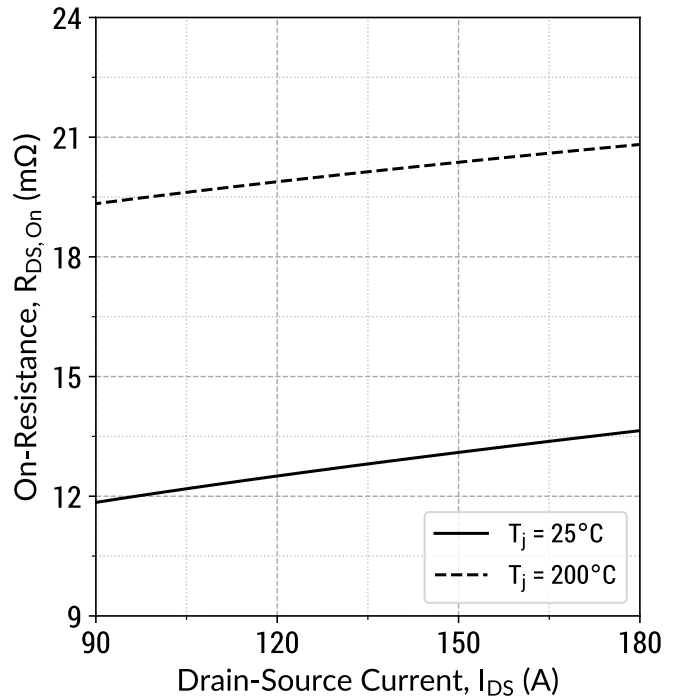
$$I_D = f(V_{GS}, T_j); t_P = 100 \mu\text{s}$$

Figure 5: On-State Resistance v/s Temperature



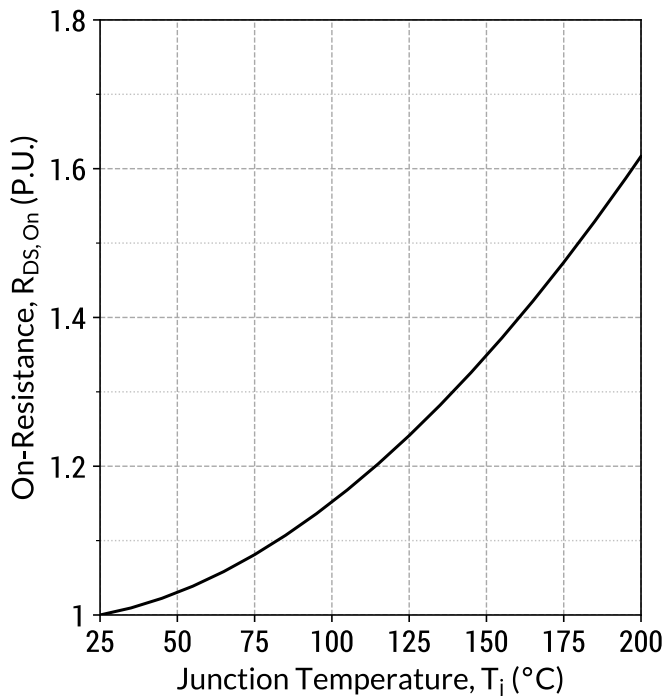
$R_{DS(on)} = f(T_j, V_{GS}); t_P = 250\ \mu\text{s}; I_D = 100\ \text{A}$

Figure 6: On-State Resistance v/s Drain Current



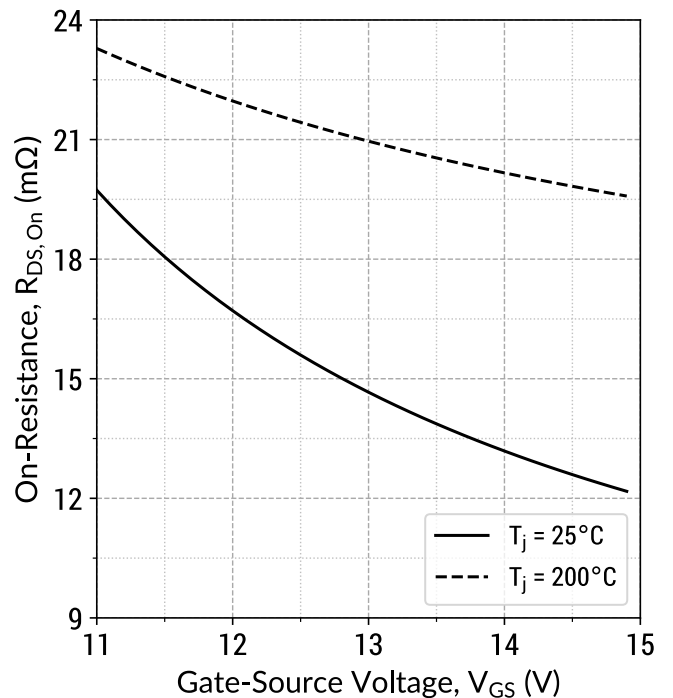
$R_{DS(on)} = f(T_j, I_D); t_P = 250\ \mu\text{s}; V_{GS} = 15\ \text{V}$

Figure 7: Normalized On-State Resistance v/s Temperature



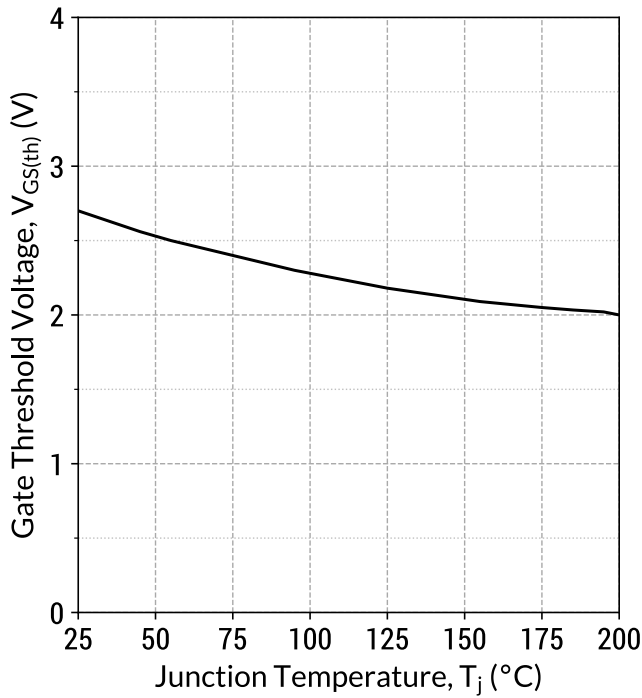
$R_{DS(on)} = f(T_j); t_P = 250\ \mu\text{s}; I_D = 100\ \text{A}; V_{GS} = 15\ \text{V}$

Figure 8: On-State Resistance v/s Gate Voltage



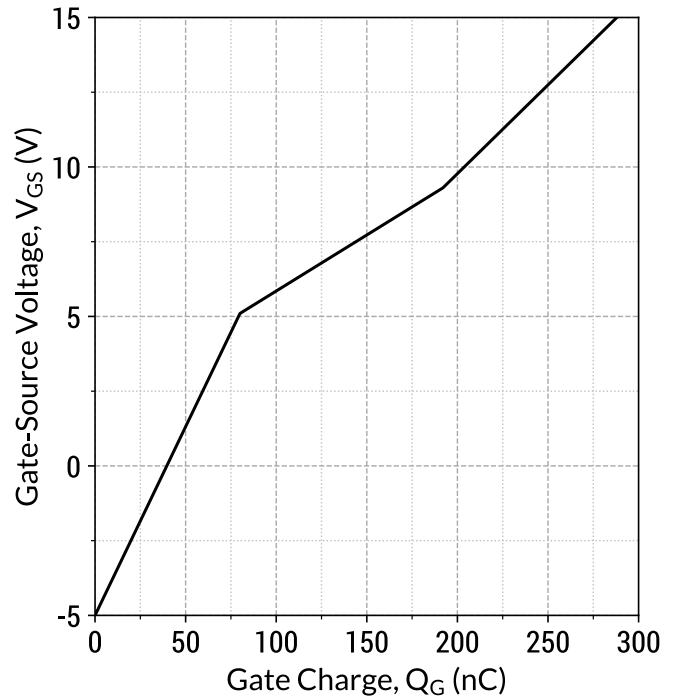
$R_{DS(on)} = f(T_j, V_{GS}); t_P = 250\ \mu\text{s}; I_D = 100\ \text{A}$

Figure 9: Threshold Voltage Characteristics



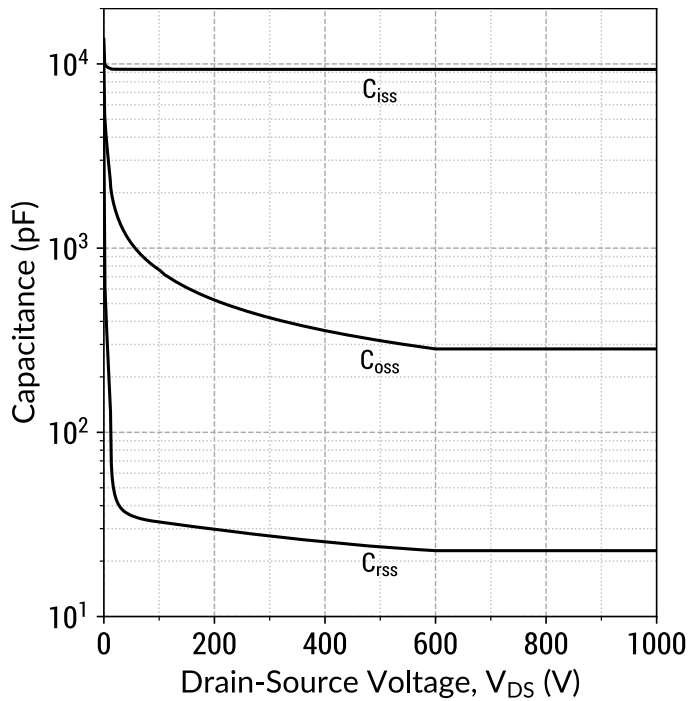
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 50.0 \text{ mA}$

Figure 10: Gate Charge Characteristics



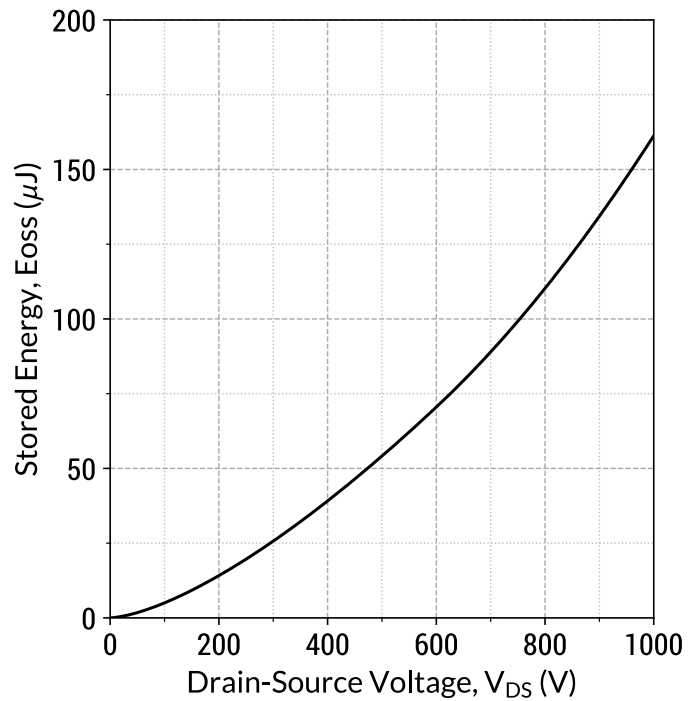
$I_D = 100 \text{ A}; V_{DS} = 800 \text{ V}; T_C = 25^\circ\text{C}$

Figure 11: Capacitance v/s Drain-Source Voltage



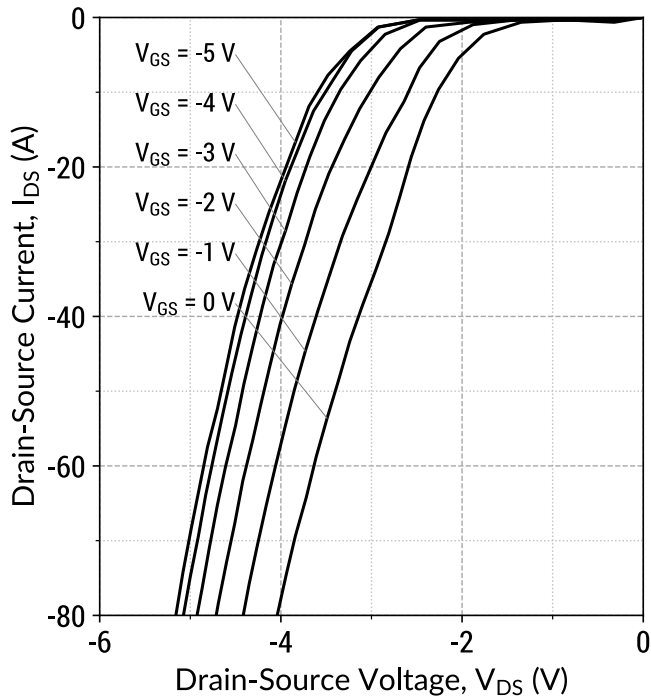
$f = 1 \text{ MHz}; V_{AC} = 25 \text{ mV}$

Figure 12: Output Capacitor Stored Energy



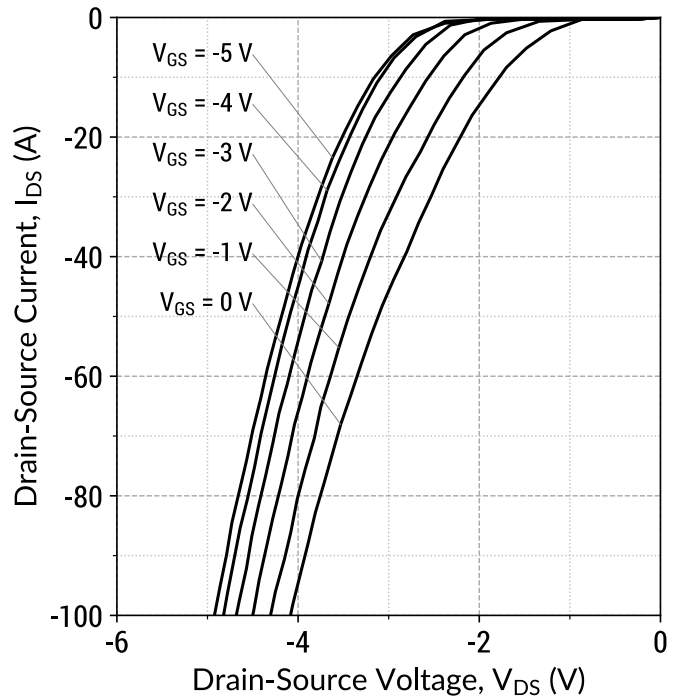
$E_{oss} = f(V_{DS})$

Figure 13: Body Diode Characteristics ($T_j = 25^\circ\text{C}$)



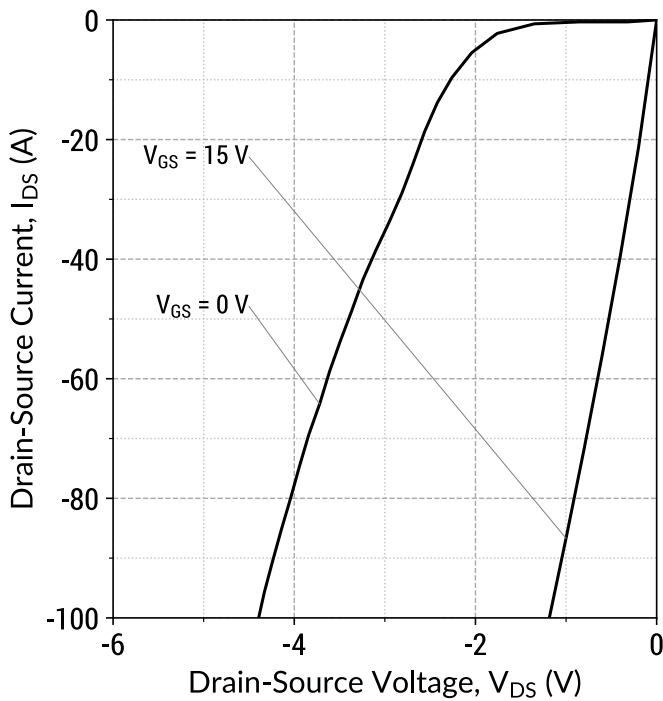
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 14: Body Diode Characteristics ($T_j = 200^\circ\text{C}$)



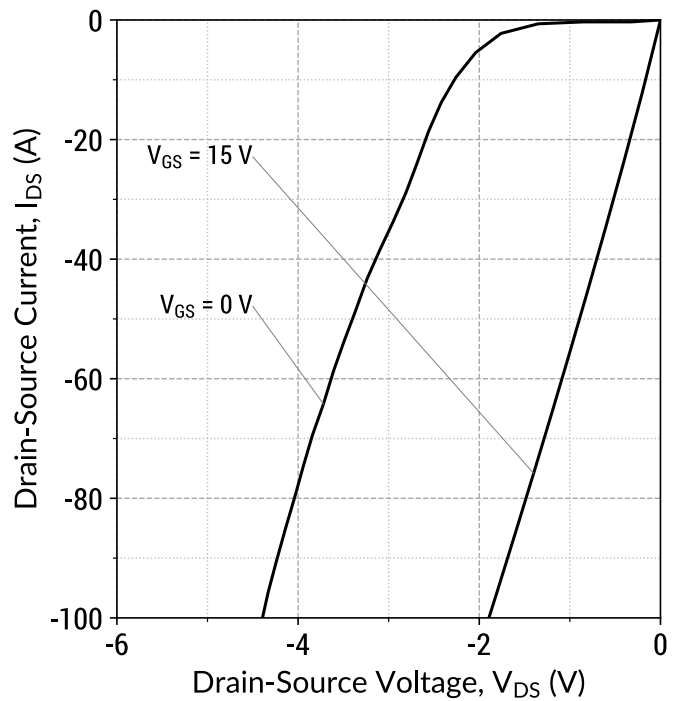
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 15: Third Quadrant Characteristics ($T_j = 25^\circ\text{C}$)



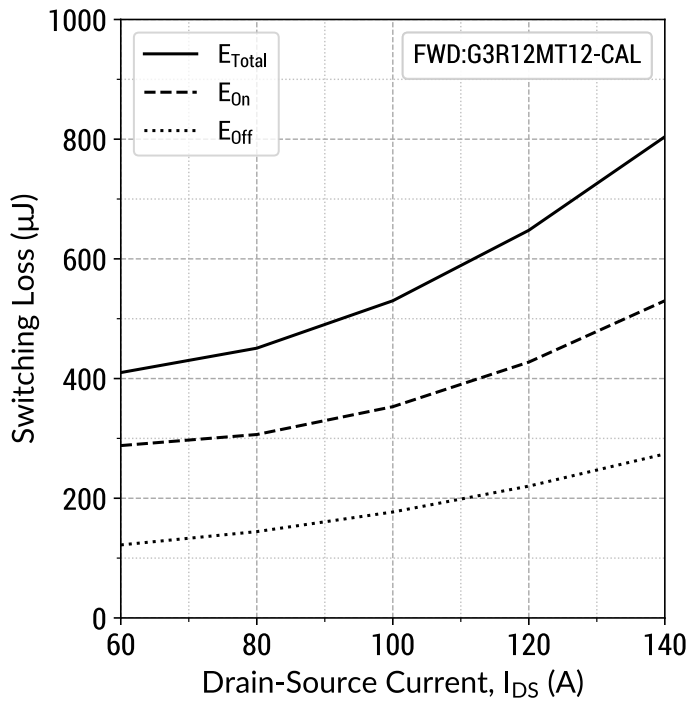
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 16: Third Quadrant Characteristics ($T_j = 200^\circ\text{C}$)



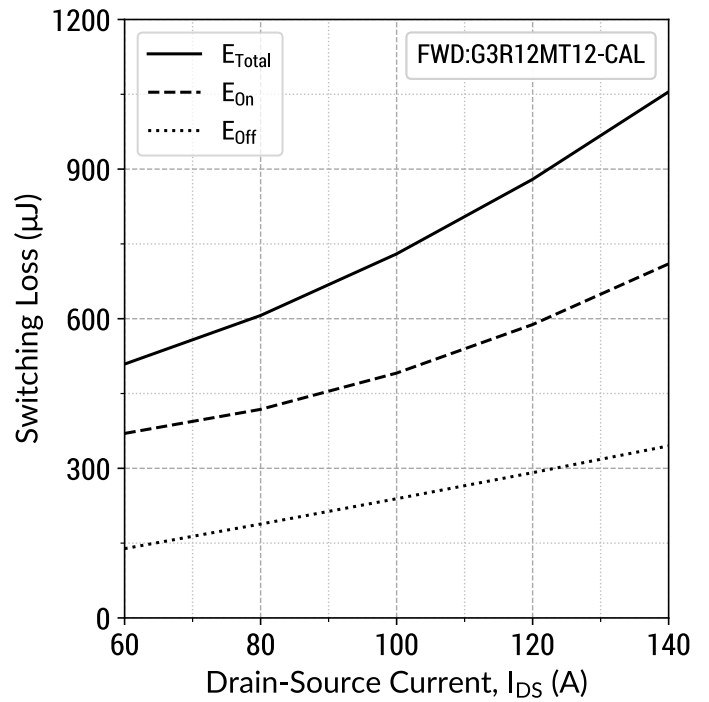
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 17: Resistive Switching Energy v/s Drain Current
($V_{DD} = 600V$)



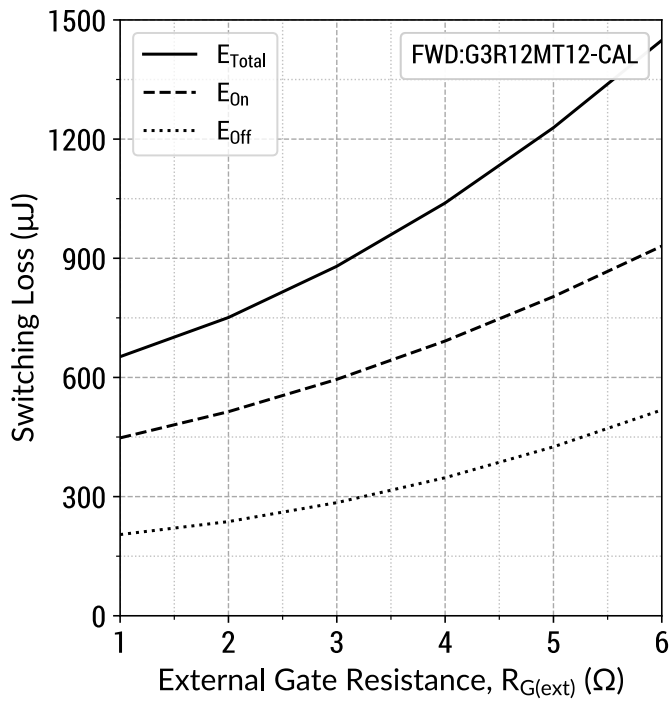
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $R_{G(ext)} = 2 \Omega$

Figure 18: Resistive Switching Energy v/s Drain Current
($V_{DD} = 800V$)



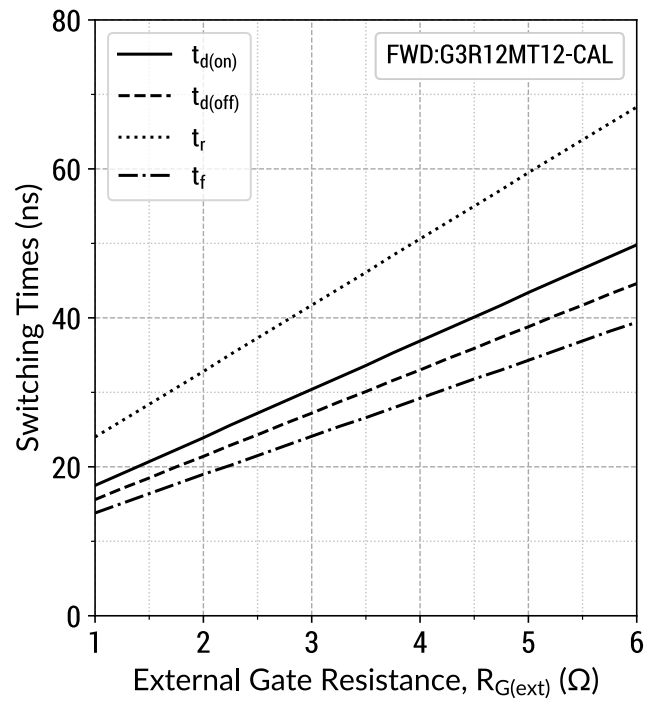
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $R_{G(ext)} = 2 \Omega$

Figure 19: Resistive Switching Energy v/s $R_{G(ext)}$
($V_{DD} = 800V$)



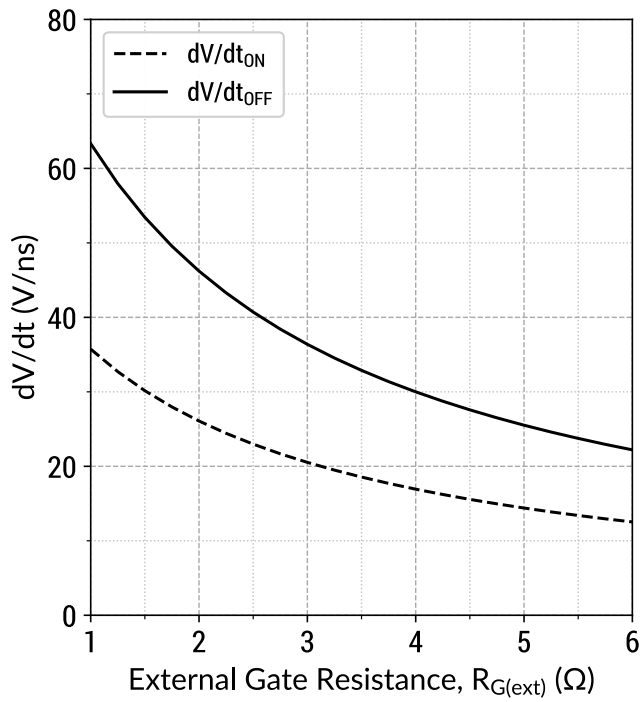
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 100 A$

Figure 20: Switching Time v/s $R_{G(ext)}$
($V_{DD} = 800V$)



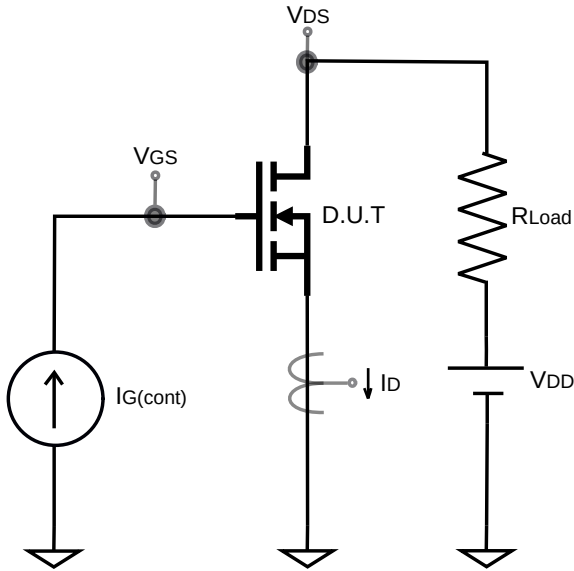
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 100 A$

Figure 21: dV/dt v/s $R_{G(ext)}$
($V_{DD} = 800V$)

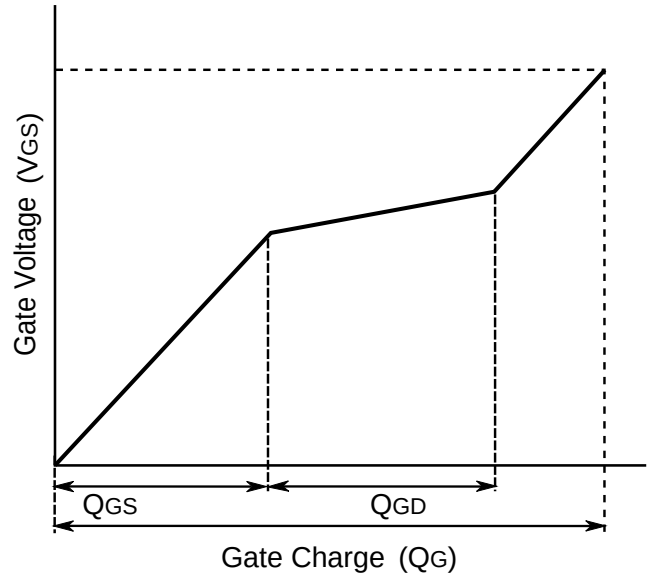


$T_J = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 100 A$

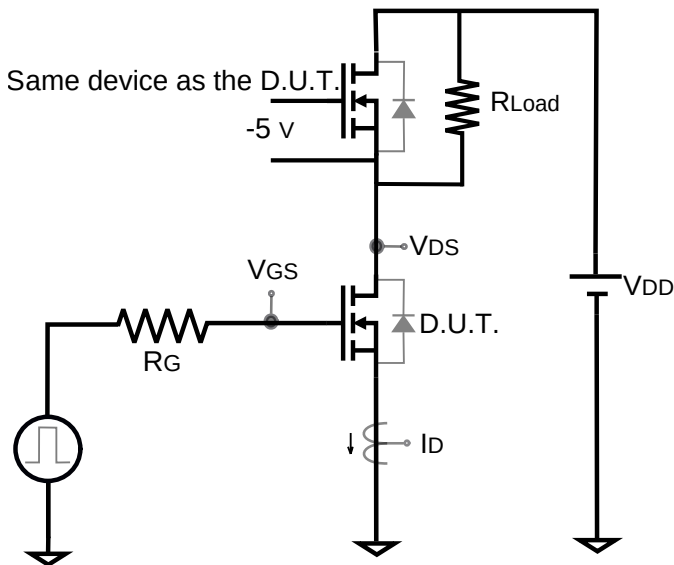
Gate Charge Circuit



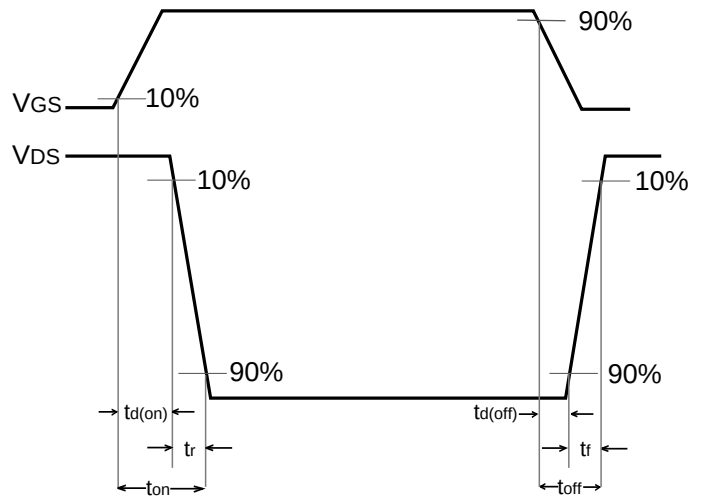
Gate Charge Waveform



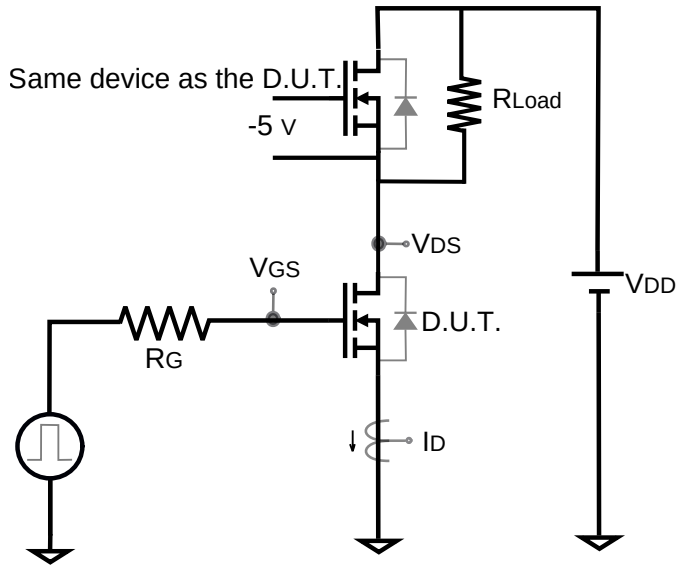
Switching Time Circuit



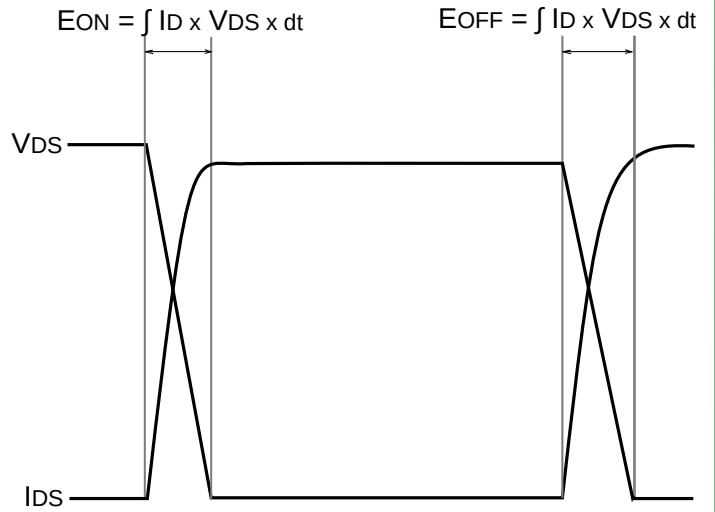
Switching Time Waveform



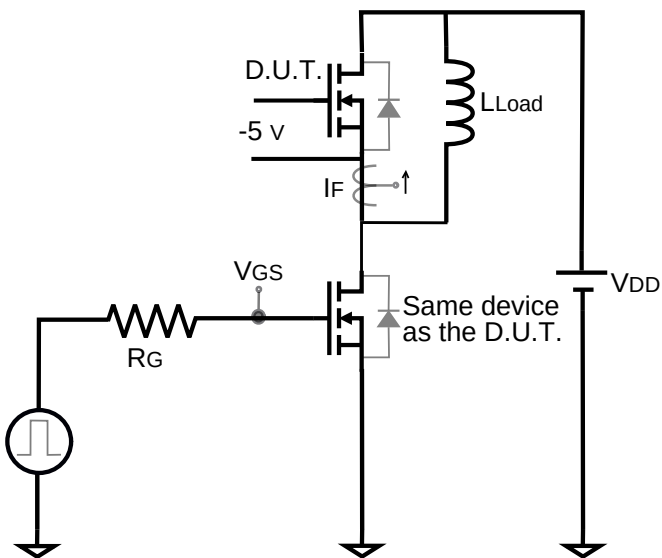
Switching Energy Circuit



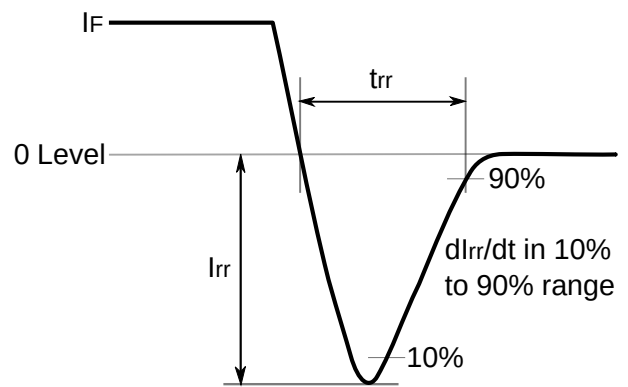
Switching Energy Waveform



Reverse Recovery Circuit



Reverse Recovery Waveform



Mechanical Parameters

This information is **confidential**, please contact sales@genesicsemi.com to learn more.

Chip Dimensions

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NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R12MT12-CAL/G3R12MT12-CAL_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R12MT12-CAL/G3R12MT12-CAL_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R12MT12-CAL/G3R12MT12-CAL_3D.zip
- Gate Driver Reference: <https://www.genesicsemi.com/technical-support>
- Evaluation Boards: <https://www.genesicsemi.com/technical-support>
- Reliability: <https://www.genesicsemi.com/reliability>
- Compliance: <https://www.genesicsemi.com/compliance>
- Quality Manual: <https://www.genesicsemi.com/quality>

Revision History

- Rev 21/Aug: Initial Release



www.genesicsemi.com/sic-mosfet/

