G2R325MS65-CAL
6500 V 325 mΩ SiC MOSFET

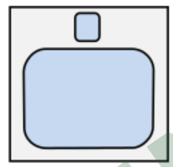
Silicon Carbide MOSFET with Integrated Schottky Diode
N-Channel Enhancement Mode

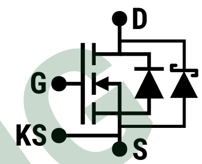
V_{DS}	=	6500 V
$R_{DS(ON)(Typ.)}$	=	325 mΩ
I_D (T_C = 115°C)	=	10 A

Features

- G2R™ Technology - +20 V / -5 V Gate Drive
- Superior Q_G x $R_{DS(ON)}$ Figure of Merit
- Low Capacitances and Low Gate Charge
- Normally-Off Stable Operation up to 175°C
- Fast and Reliable Integrated Schottky Diode
- High Avalanche and Short Circuit Ruggedness
- Low Conduction Losses at High Temperatures

Bare Chip





D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS

REACH

Advantages

- Increased Power Density for Compact System
- High Frequency Switching
- Reduced Losses for Higher System Efficiency
- Minimized Gate Ringing
- Improved Thermal Capability
- Superior Cost-Performance Index
- Ease of Paralleing without Thermal Runaway
- Simple to Drive

Applications

- High Voltage Converters
- Smart Grid and HVDC
- Traction
- Pulsed Power

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	6500	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +25	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +20	V	
Continuous Forward Current	I_D	T_C = 25°C, V_{GS} = -5 / +20 V	15	A	Note. 2
		T_C = 100°C, V_{GS} = -5 / +20 V	11		
		T_C = 135°C, V_{GS} = -5 / +20 V	8		
Power Dissipation	P_D	T_c = 25°C	315	W	Note. 2
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

Note 2: Assuming $Rth_{JC(max)}$ = 0.48°C/W(insulated base-plate package)

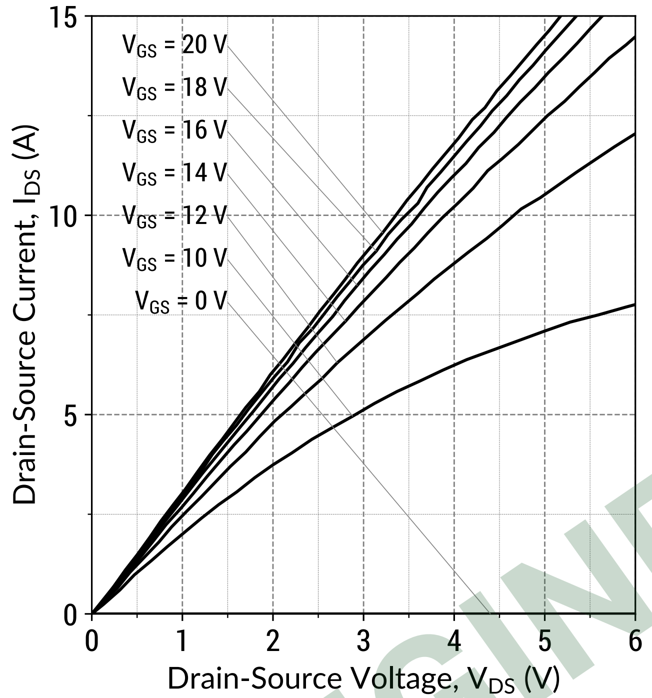
Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	6500			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 6500 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 25 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 6.0 mA V_{DS} = V_{GS}, I_D = 6.0 mA, T_j = 175°C		2.7 1.71		V	Fig. 9
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 5 A V_{DS} = 10 V, I_D = 5 A, T_j = 175°C		2.5 2.6		S	Fig. 4
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 20 V, I_D = 5 A V_{GS} = 20 V, I_D = 5 A, T_j = 175°C		325 1080	406	mΩ	Fig. 5-8
Input Capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V f = 1 MHz, V_{AC} = 25mV		3395		pF	Fig. 10
Output Capacitance	C_{oss}			80		pF	Fig. 10
Reverse Transfer Capacitance	C_{rss}			12.7		pF	Fig. 10
C_{oss} Stored Energy	E_{oss}			31		µJ	Fig. 11
C_{oss} Stored Charge	Q_{oss}			110		nC	
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		2		Ω	

Reverse Diode Characteristics

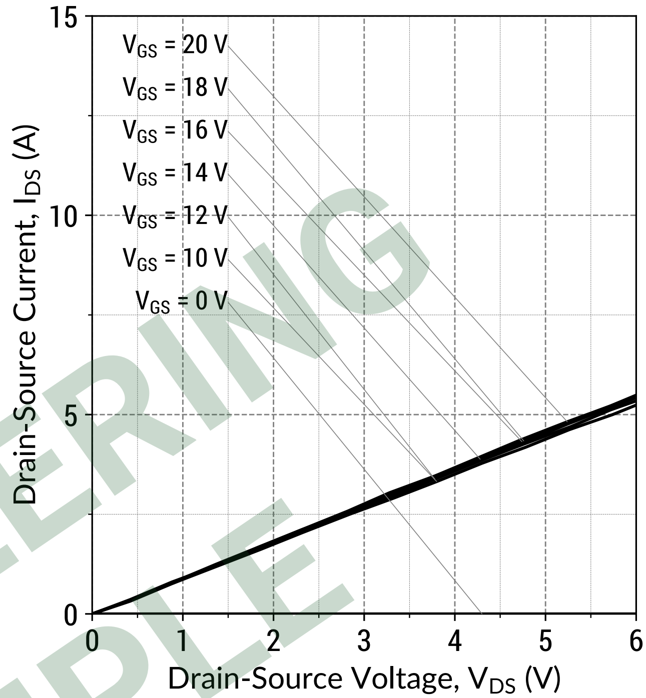
Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 5 A V_{GS} = -5 V, I_{SD} = 5 A, T_j = 175°C		3.3 4.3		V	Fig. 12-13

Figure 1: Output Characteristics (T_j = 25°C)



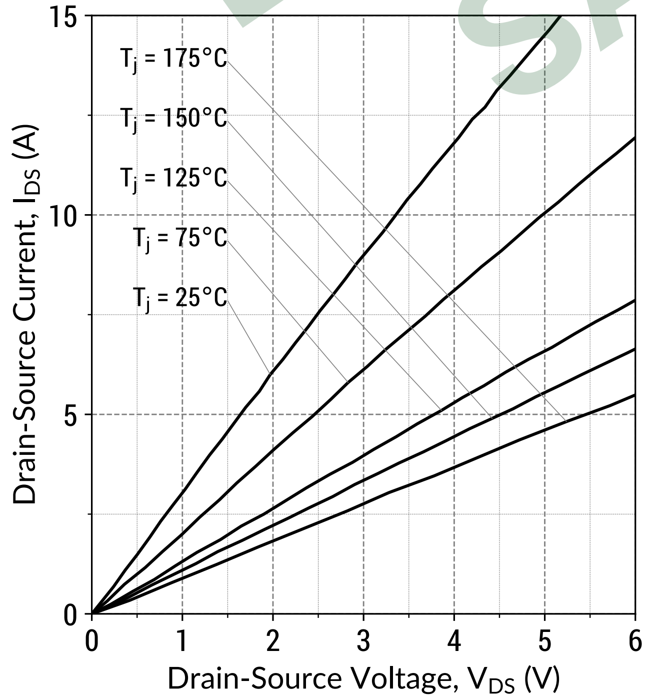
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 2: Output Characteristics (T_j = 175°C)



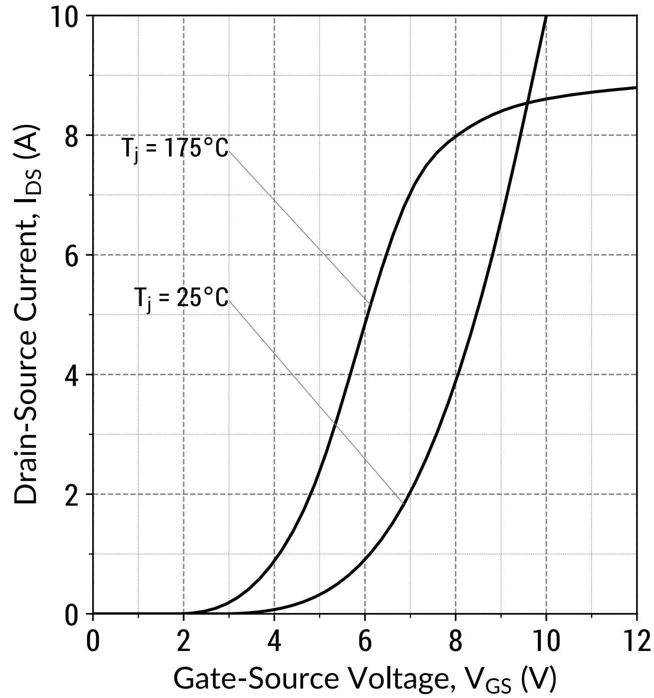
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 3: Output Characteristics (V_{GS} = 20 V)



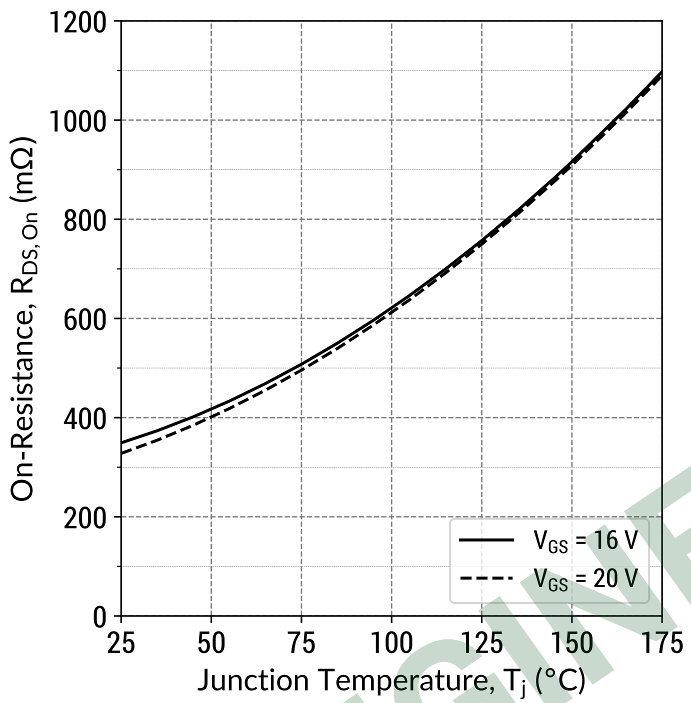
$I_D = f(V_{DS}, T_j)$; t_P = 250 µs

Figure 4: Transfer Characteristics (V_{DS} = 10 V)



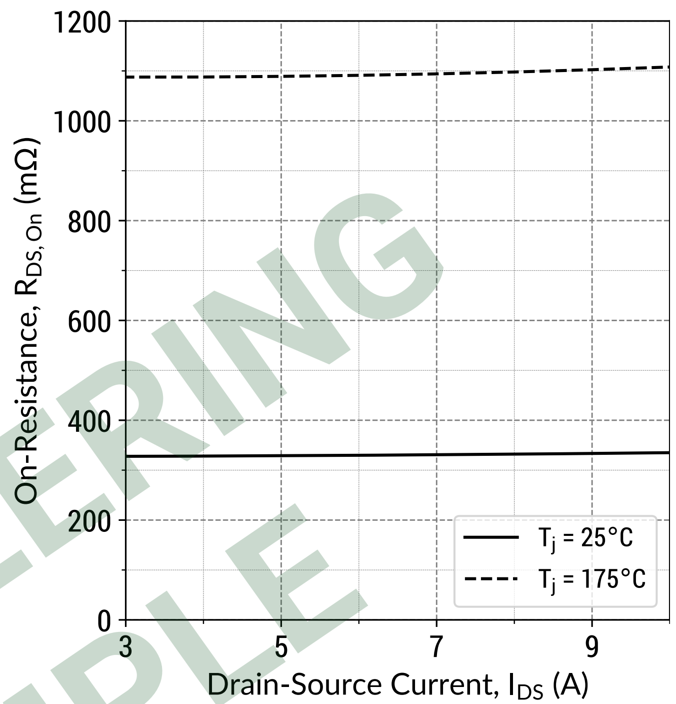
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Figure 5: On-State Resistance v/s Temperature



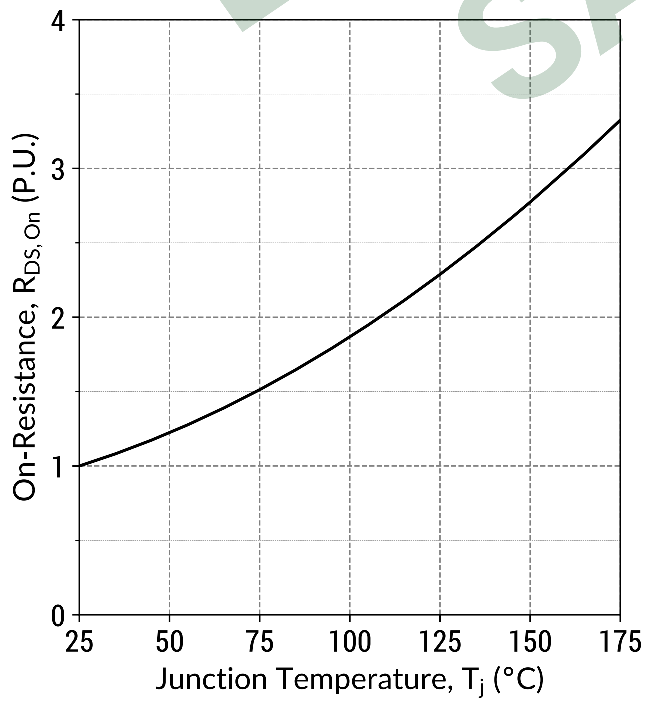
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 5 A

Figure 6: On-State Resistance v/s Drain Current



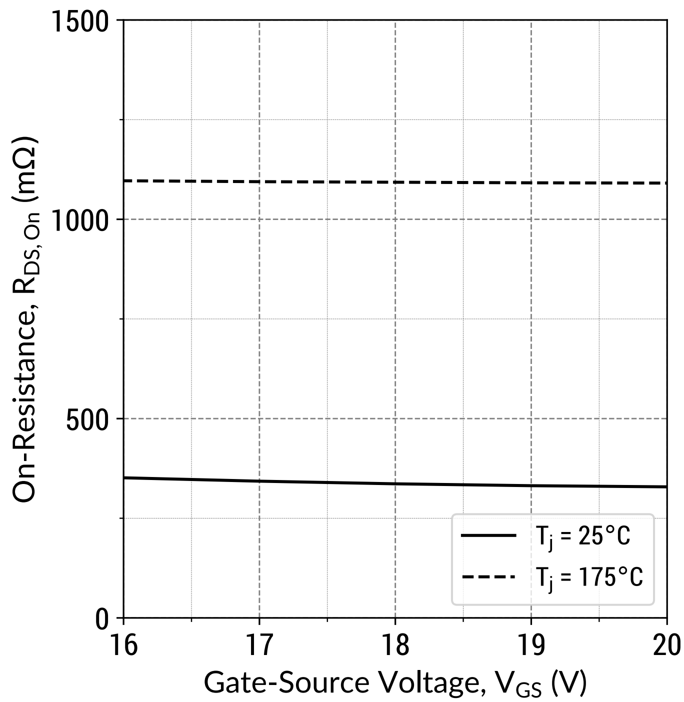
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 250 µs; V_{GS} = 20 V

Figure 7: Normalized On-State Resistance v/s Temperature



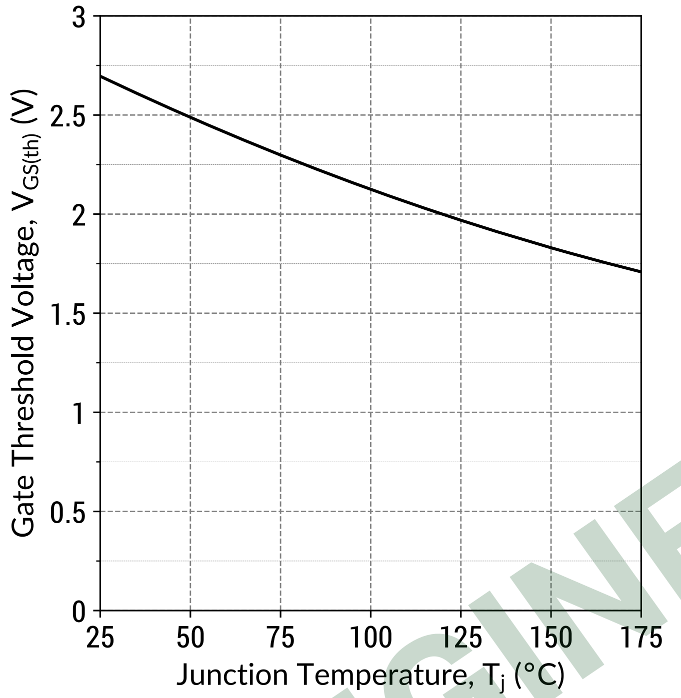
$R_{DS(ON)} = f(T_j)$; t_P = 250 µs; I_D = 5 A; V_{GS} = 20 V

Figure 8: On-State Resistance v/s Gate Voltage



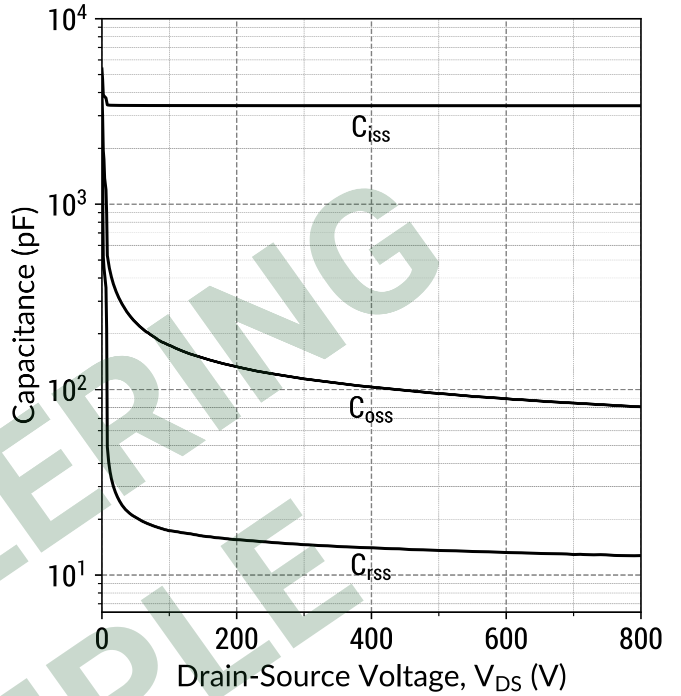
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 5 A

Figure 9: Threshold Voltage Characteristics



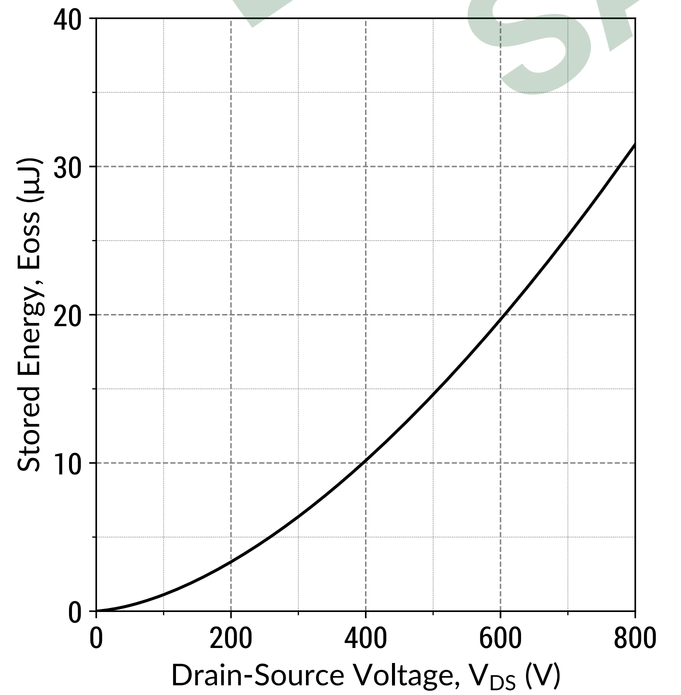
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; I_D = 6.0 mA

Figure 10: Capacitance v/s Drain-Source Voltage



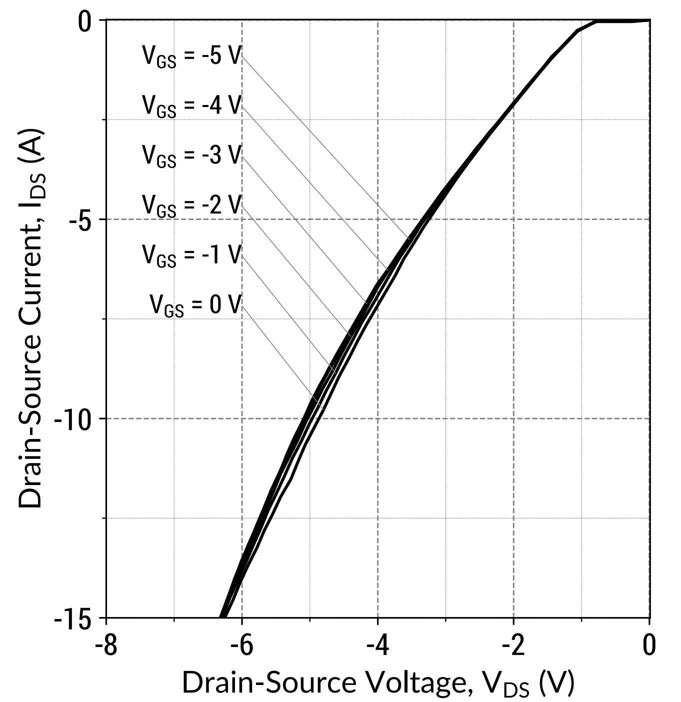
f = 1 MHz; V_{AC} = 25mV

Figure 11: Output Capacitor Stored Energy



$E_{oss} = f(V_{DS})$

Figure 12: Body Diode Characteristics (T_j = 25°C)



$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

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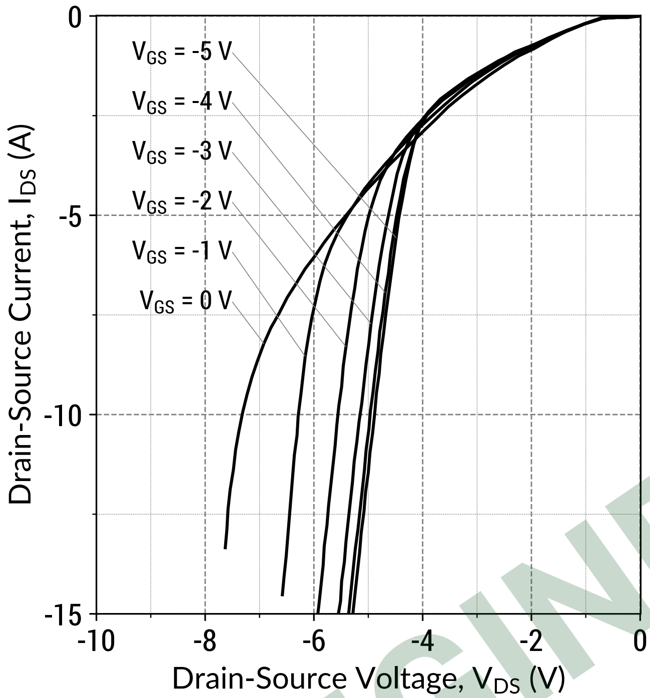
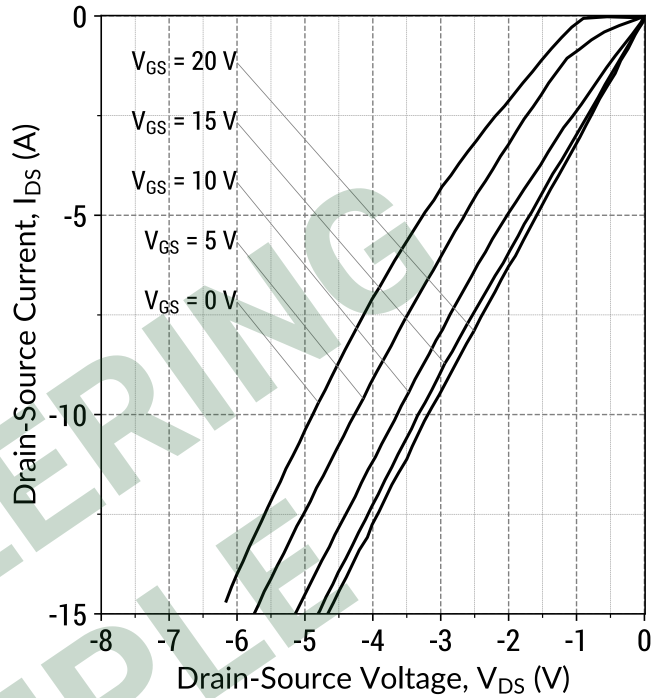
Figure 13: Body Diode Characteristics (T_j = 175°C)



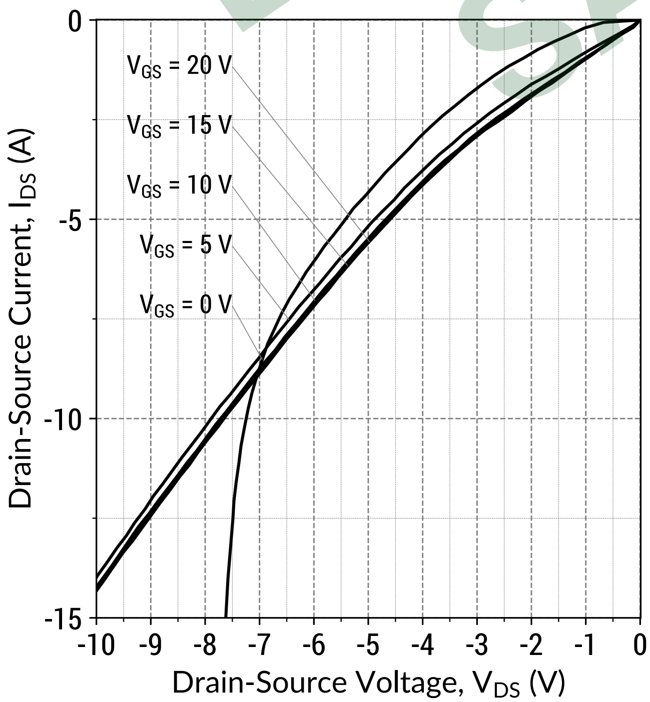
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 14: Third Quadrant Characteristics (T_j = 25°C)



$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 15: Third Quadrant Characteristics (T_j = 175°C)



$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Mechanical Parameters

This information is confidential, please contact **sales@genesicsemi.com** to learn more.

Chip Dimensions

This information is confidential, please contact **sales@genesicsemi.com** to learn more.

NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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- Gate Driver Reference: https://www.genesicsemi.com/technical-support
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- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

Revision History

Date	Revision	Comments	Supersedes
Sep. 28, 2020	Rev 1	Initial Release	

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Published by GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155, Dulles, VA 20166; USA