Correlation between carrier recombination lifetime and forward voltage drop in 4H-SiC PiN diodes

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Abstract. Correlation between carrier lifetime and forward voltage drop in 4H-SiC PiN diodes has been investigated. PiN diodes from the drift layer of 20 μm shows breakdown voltage of 3.3 kV and forward voltage drop as low as 3.13 V at 100A/cm^2. Variation of calculated forward voltage drop (V_F) from measured carrier lifetimes is very comparable to measured V_F of fully processed PiN diodes. Measured carrier lifetime and V_F of PiN diodes also show good spatial correlation. Wafer level lifetime mapping can be employed to assess and predict V_F of PiN diodes.

Introduction

Silicon Carbide is the material of choice for high-voltage, fast-switching, and high-temperature applications because of its wide bandgap energy, large critical electric field and high thermal conductivity [1]. Bipolar devices can achieve lower power dissipation than unipolar devices in high voltage application areas due to its conductivity modulation effect. Conductivity modulation of the base layer of bipolar devices determines on-state resistance and strongly depends on carrier recombination lifetimes of the layer. To realize bipolar switching rectifiers, understanding dominant lifetime control mechanisms and developing a convenient wafer mapping technique for SiC are key factors. Recently, μ-PCD (microwave photoconductive decay) with full wafer mapping capability was demonstrated for both n- and n-/p+ wafers and showed full lifetime wafer maps can be used for an epitaxial wafer quality metric [2,3]. In this work, wafer level carrier lifetime data and the electrical characteristics of PiN rectifiers are analyzed and direct correlation between carrier recombination lifetime and forward bias drop is presented.

Experiment

The starting materials are 3” SiC epitaxial PiN wafers grown by a planetary warm wall reactor from chlorosilane/propane chemistry SiC substrates with drift doping of 1.5x10^{15}/cm^3 and thickness at 20 μm with continuous p+ growths (2 μm). μ-PCD measurements were performed at room temperature before device processing. Details of μ-PCD measurements are given in [2]. Typical lifetime measured on the PiN epi layer configuration was about 0.9 μs. PiN diodes were fabricated with mesa by reactive ion etching (RIE) and a single zone JTE by boron implant and

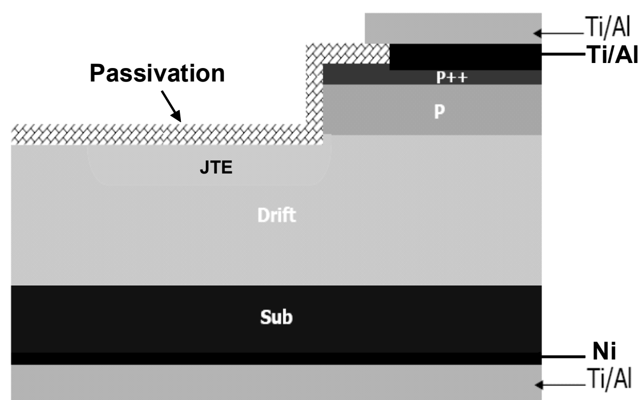

Fig. 1 Schematic illustration of a PiN diode

activation annealing at 1700 °C. Ti-Al and Ni were used to form ohmic contacts to the anode and cathode regions, respectively. Rapid thermal annealing was used for alloying the ohmic contacts. Fig. 1 shows schematic illustration of SiC PiN diode. Active device design consists of a circular layout with diameters of 0.25, 0.5 and 1 mm. All electrical measurements were performed on unpackaged devices.

Results and discussion

Fig. 2 shows a linear current density-voltage (J-V) characteristic obtained from a representative 1 mm-diameter diode at room temperature. Variations of the critical field and the breakdown voltage as a function of drift layer doping at the drift layer thickness of 20 μm are calculated with the punch through diode model for 4H-SiC (fig. 2(b)). For the drift layer of $1.5 \times 10^{15}/cm^3$ in this work, a critical electric field of 2.05 MV/cm can be expected at breakdown voltage at 3.55 kV [4]. The diode blocked a very high voltage of 3.3 kV. This experimentally measured breakdown voltage is about 94% of the ideal parallel plane breakdown voltage.

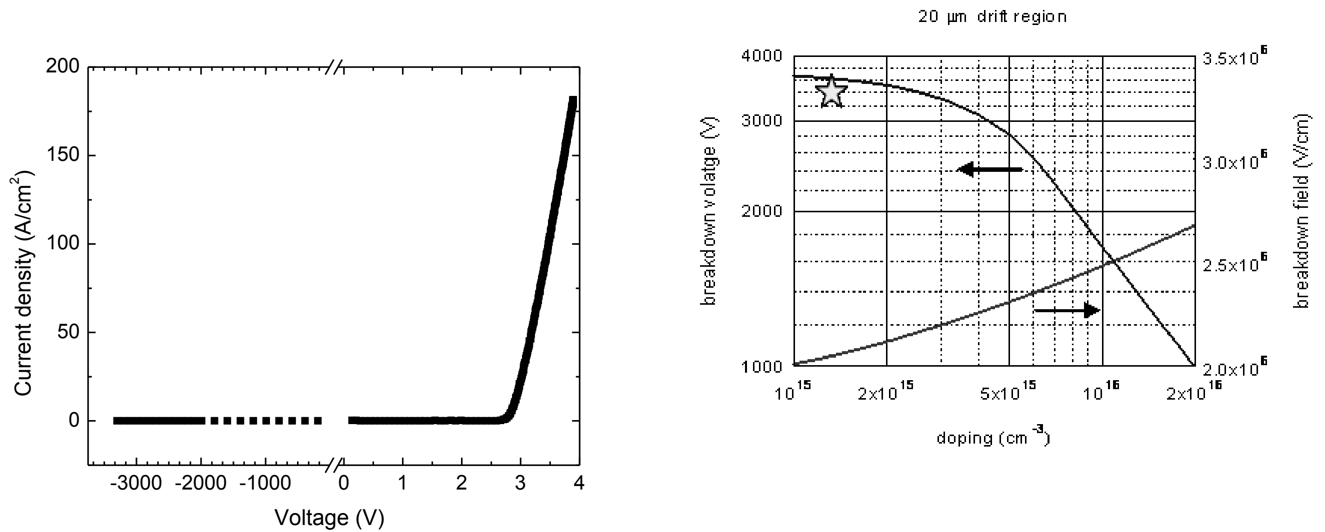

Fig. 2. Linear J-V characteristics of SiC PiN diode at room temperature (a). Theoretical critical electric field and breakdown voltage values as a function of the doping of 20 μm drift layer (b). Star represents the best diode in this work.

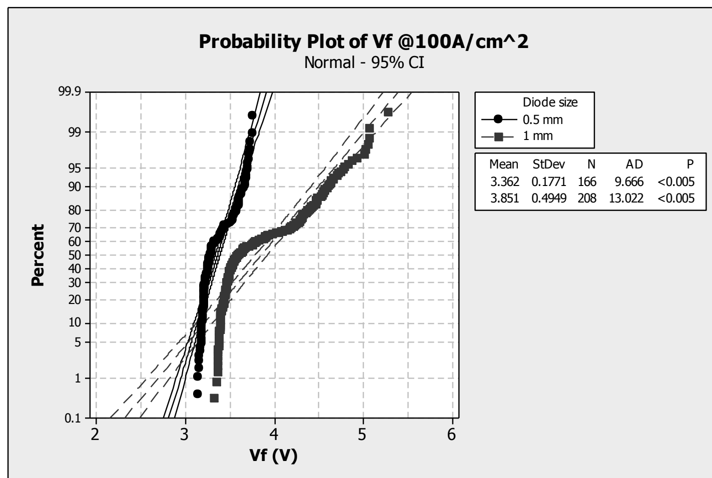

Fig. 3. Probability plot of V_F at $100 A/cm^2$ for the diodes of 0.5 and 1mm diameter from the wafers (AN5042-03 and AQ5026-02).

Fig 3 shows probability plot of V_F from 0.5 and 1 mm diameter diodes. On-state voltage drops as low as 3.13 V and 3.3 V at a forward current of $100 A/cm^2$ are measured for the 0.5 and 1 mm diameter diodes, respectively. The difference results from more efficient current spreading at 0.5 mm diodes. Differential on-resistance extracted from forward J-V curves shows a value as low as 2.5 $m\Omega cm^2$ from 0.5 mm diameter diodes. These low V_F values in conjunction with the high blocking voltages are an indication of the starting material quality as well as the device process and design strategy. It has been experimentally observed that chlorosilane based CVD epitaxy layers have lower vacancy

defects, which are responsible for reduction of lifetimes [5]. It is previously reported that measured effective recombination lifetime values decrease significantly in the presence of the p^+/n^- interface relative to that measured on wafers with n- drift layer alone [3]. Some discrepancies have been also reported between electrically and optically measured lifetimes in PiN structures [6]. Thus, it is critical to understand which lifetimes represent on-state characteristics of PiN diodes to predict forward device performance of PiN diodes before device processing. On wafer-level lifetime measurements were performed on fully grown PiN structure eptaxy wafers at room temperature before device processing with an example shown in fig. 4. Within wafer average and uniformity (sigma/mean) values of lifetimes are 0.85 μs and 35%, respectively. Edge of the wafer shows relatively lower lifetimes. Some blank sites (white color coded) are from very low microwave signal strength and can be related with macro material defects like grain-boundaries or polytype switching areas.

Fig. 4. Lifetime wafer map from a PiN structure epitaxy wafer. This wafer has been used to produce PiN diodes in fig. 2 and 3.

The on-state voltage drop in a PIN diode can be written as the sum of the voltage drops in the drift layer (V_M), p+ contact (V_{p_+}), substrate (V_{subs}) and the p+/n and n+/n junctions ($V_{P^+N^-} + V_{N^+N^-}$):

$$V_F = V_{p+} + V_M + V_{P^+N^-} + V_{N^+N^-} + V_{subs} \quad (1)$$

$V_{P^+N^-} + V_{N^+N^-}$ can be estimated to be equal to the turn-on voltage of the SiC P+N+ junction and a simple calculation yields 3.1 V [7]. V_M is determined by the extent of conductivity modulation in the drift layer and is dependent on the carrier lifetime by following relationship.

$$V_M = \frac{3kT}{q}\left(\frac{W}{2L_a}\right)^2 \quad \text{for } W \le 2L_a \quad (2)$$

$$V_M = \frac{3\pi kT}{8q} e^{W/L_a} \quad \text{for } W \ge 2L_a \quad (3)$$

Where W is drift layer thickness and L_a is the ambipolar diffusion length. $L_a = \sqrt{D\tau}$ and D is ambipolar diffusion constant and τ is carrier recombination lifetime at high injection level. It is important to note that V_M is independent of the current density. As the half of W becomes longer than the diffusion length, V_M causes an appreciable increase in the forward voltage drop due to a reduction in the conductivity modulation in the central portion of the drift layer. D was about 2.3 cm^2/s in 4H-SiC at high injection level [8]. Calculated V_M with the boundary conditions above and lifetimes measured by μ-PCD ranges from 0.02 to 0.83 V. Calculated V_F at the average lifetime of 0.85 μs is close to the turn on voltage of the p+/n and n+/n junctions ($V_{P^+N^-} + V_{N^+N^-}$) since calculated V_M is only about 0.05 V and calculated L_a is longer than the half of the drift layer thickness. The lowest liftime vaule of 0.16 μS results in calculated V_F of 3.9 V, which is comparable to the highest tested V_F with 0.5 mm diodes. To see spatial correlation between measured lifetimes and V_F of processed PiN diodes, lifetime and V_F wafer distributions are compared using wafer maps. Diodes are grouped as four bins in terms of V_F and then

recombination lifetimes are tabulated from those devices. Fig. 5 shows boxplots of V_F @ 50 and 100A/cm^2 with measured lifetimes. It is clear that longer lifetimes result in lower V_F in PiN diodes. Some variations in each bin might be related with error of site registeration from wafer maps and variations in V_{p_+} and V_{subs}. Good spatial correlation and comparable variations between measured V_F and measurd lifetimes suggest that wafer level lifetime time testing can predict V_F of fully processed PiN diodes.

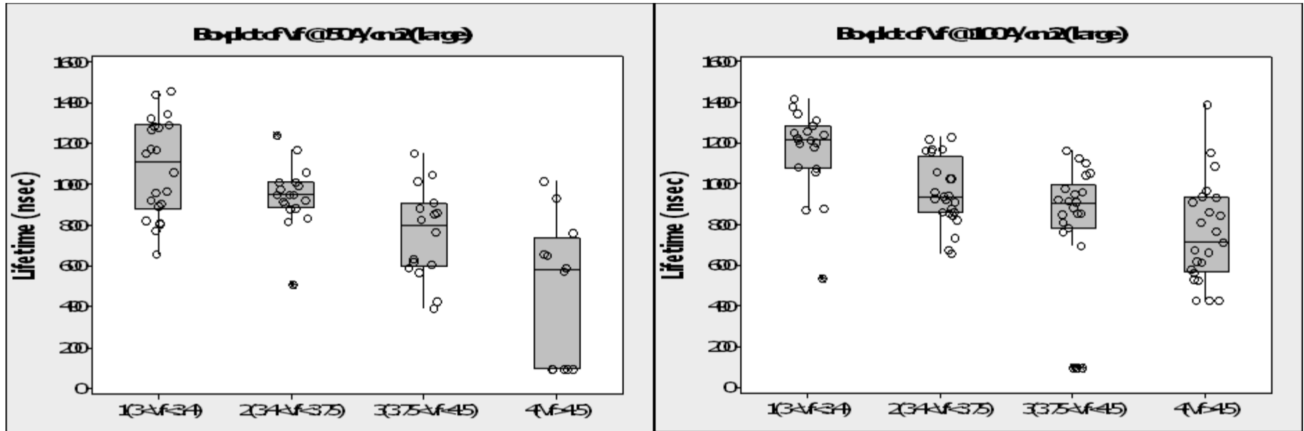

Fig. 5 Boxplots of lifetimes from four groups of V_F at 50 and 100 A/cm^2

Summary

PiN diodes from the drift layer of 20 μm show the breakdown voltage of 3.3 kV and on-state voltage drop as low as 3.13 V at 100A/cm^2. These good results are indication of a good starting material quality as well as optimized SiC process conditions. Wafer level carrier lifetimes are measured from fully grown PiN structures by μ-PCD. Variations of V_M calculated with measured carrier lifetimes are very comparable to measured V_F of PiN diodes. It is observed that measured lifetimes and measured V_F show good spatial correlation and longer lifetimes result in lower V_F.

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