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Introductory Invited Paper

Reliability and performance limitations in SiC power devices

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Abstract

Despite silicon carbide's (SiC's) high breakdown electric field, high thermal conductivity and wide bandgap, it faces certain reliability challenges when used to make conventional power device structures like power MOS-based devices, bipolar-mode diodes and thyristors, and Schottky contact-based devices operating at high temperatures. The performance and reliability issues unique to SiC discussed here include: (a) MOS channel conductance/gate dielectric reliability trade-off due to lower channel mobility as well as SiC–SiO_2 barrier lowering due to interface traps; (b) reduction in breakdown field and increased leakage current due to material defects; and (c) increased leakage current in SiC Schottky devices at high temperatures.

Although a natural oxide is considered a significant advantage for realizing power MOSFETs and IGBTs in SiC, devices to date have suffered from poor inversion channel mobility. Furthermore, the high interface state density presently found in the SiC–SiO_2 system causes the barrier height between SiC and SiO_2 to be reduced, resulting in increased carrier injection in the oxide. A survey of alternative dielectrics shows that most suffer from an even smaller conduction band offset at the SiC–dielectric interface than the corresponding Silicon–dielectric interface and have a lower breakdown field strength than SiO_2. Thus, an attractive solution to reduce tunneling such as stacked dielectrics is required.

In Schottky-based power devices, the reverse leakage currents are dominated by the Schottky barrier height, which is in the 0.7–1.2 eV range. Because the Schottky leakage current increases with temperature, the SiC Schottky devices have a reduction in performance at high temperature similar to that of Silcon PN junction-based devices, and they do not have the high temperature performance benefit associated with the wider bandgap of SiC.

Defects in contemporary SiC wafers and epitaxial layers have also been shown to reduce critical breakdown electric field, result in higher leakage currents, and degrade the on-state performance of devices. These defects include micropipes, dislocations, grain boundaries and epitaxial defects. Optical observation of PN diodes undergoing on-state degradation shows a simultaneous formation of mobile and propagating crystal stacking faults. These faults nucleate at grain boundaries and permeate throughout the active area of the device, thus degrading device performance after extended operation.

1. Introduction

Evolutionary improvements in silicon power devices through better device designs, processing techniques and material quality have led to great advancements in power systems in the last four decades. However, many

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commercial power devices are now approaching the theoretical performance limits offered by the silicon (Si) material in terms of the capability to block high voltage, provide low on-state voltage drop, and switch at a high frequency. Therefore, in the past 5–6 years, many power system designers have been looking for alternative solutions in order to realize advanced commercial and military hardware that requires higher power density circuits and modules. One of the most promising approaches is to replace Si as the material of choice for fabrication of power devices with a wider bandgap material with acceptable bulk mobility [1]. A revolution is now underway to exploit the excellent properties of silicon carbide (SiC) for the realization of high performance, next generation power devices. These material properties include: (a) an order of magnitude higher breakdown electric field; (b) a ~3× wider bandgap; and (c) a ~3× higher thermal conductivity than silicon. A high breakdown electric field allows the design of SiC power devices with thinner and higher doped blocking layers. The large bandgap of SiC results in a much higher operating temperature and higher radiation hardness. The high thermal conductivity for SiC (4.9 °C/W) allows dissipated heat to be more readily extracted from the device. Hence, a larger power can be applied to the device for a given junction temperature. Although many devices utilizing these benefits have been demonstrated, the long term reliability issues of various device structures have received relatively little attention. This paper addresses the reliability issues faced by contemporary SiC power devices.

As in Si, SiC power devices may be broadly classified into majority carrier devices, which primarily rely on drift current during on-state conduction; and minority carrier devices (also called bipolar-type devices), which result in conductivity modulation during on-state operation. Majority carrier devices like the Schottky diodes, power MOSFETs and JFETs offer extremely low switching power losses because of their high switching speed. Although the on-state (forward) voltage drop of majority carrier devices can be low, it becomes prohibitively high at high current densities. This problem exponentially increases in its severity as the voltage rating on power devices is increased. On the other hand, bipolar-type devices such as PiN diodes, IGBTs, thyristors, BJTs and field controlled thyristors offer low forward voltage drops at high current densities, but have higher switching losses than majority carrier devices. However, SiC bipolar devices suffer from a ~4× higher built-in junction voltage drop as compared to Si devices due to their larger bandgap resulting in a large forward voltage at low currents. Although the total on-state drop of SiC bipolar devices may be lower than Si devices in the ultra-high voltage regime, their full potential may be difficult to realize because conventional power device packaging technology can only dissipate 200–300 W/cm^2 continuously. Since the built-in voltage of 4H-SiC bipolar devices is ~2.8 V, the maximum continuous current may be limited to less than 100–150 A/cm^2 [2] for bipolar device types which have an odd number of p–n junctions (the built-in potential can cancel in devices with an even number of junctions).

Numerous SiC majority carrier power devices that have recently been demonstrated break the 'silicon theoretical limits' and have led to an acceleration of research and development activity. Probably the most exciting event establishing the viability of majority carrier SiC power devices is the rapid adoption of commercial SiC Schottky rectifiers in the 600 V range [3]. On a 0.64 cm^2 single chip SiC Schottky diode, a current of 130 A was demonstrated [4] using micropipe-free regions of a wafer. Junction barrier Schottky diodes with commercially attractive current capabilities have been demonstrated in the 1200–2800 V range [5,6], and may become the next commercial SiC device type. The power MOSFET in SiC is a relatively simple device type with excellent prospects as a candidate to improve and extend the capability of Si IGBTs in a wide range of applications. Even though the SiC MOS inversion layer mobility requires much research, important advances have been demonstrated in planar MOS devices. These include the demonstration of 10 V power MOSFETs [7,8] and accumulation mode MOSFETs (ACCUFET) with a low specific on-resistance of 15 mΩ cm^2 [9]. Another development in MOS-based power SiC FETs, that has resulted in a device far exceeding the theoretical performance limitations of Silicon, is the 5 kV SIAFET [10]. The SiC JFET is a majority carrier device type that does not suffer from the low MOS inversion channel mobility and high temperature gate oxide reliability challenges of the SiC MOSFETs. The highest voltage SiC-based JFET demonstrated in a practical circuit includes the 5.5 kV SEJFET [11]. Other JFETs with commercially relevant capabilities have been demonstrated with capabilities of 4 A at up to 3.3 kV [12]. In order to achieve low on-state resistance in JFETs, researchers have proposed to use a small positive bias on the gate electrode to aid the JFET channel conductance. Examples of such efforts are the 5 kV SIJFET [13], 600 V 10 A MOS-enhanced JFET [14], and the 1.7 kV JFET [15]. A novel approach proposed in the mid-90s [16] exploits the high voltage advantage of SiC-based JFETs and the mature fabrication technology and high channel mobility of a Si MOSFET in a cascode configuration. The net result is a hybrid device that offers the full functionality of a high voltage power MOSFET [17].

On-state and switching design trade-offs in bipolar devices are critically dependent on the stored charge. SiC Bipolar devices have attracted much attention for high power applications, because SiC bipolar devices have 30–100× less stored charge, and tolerate a wide temperature excursion compared to Si bipolar devices with similar voltage ratings [18]. This is because: (a)

the voltage blocking layer is an order of magnitude thinner; (b) the minority carrier lifetimes required for adequate conductivity modulation is much smaller; and (c) the doping in the blocking layers are an order of magnitude higher than comparably rated Si devices. The highest voltage functional semiconductor device reported to date is the 19.3 kV SiC PiN rectifier [19]. After a long development process [18], the highest power single chip SiC device (a PiN rectifier) was demonstrated recently with a 7.4 kV, 330 A (pulsed) capability [20]. Similar devices have been put in active circuits to show the benefits of SiC PiN rectifiers for utility applications [21]. Thyristors were among the first three-terminal bipolar switches that attracted reasonable attention because they can offer very high current density operation [22]. Recently, higher power gate turn-off thyristors (GTOs) have been demonstrated with 3–12 kV blocking capability [23,24]. Bipolar junction transistors (BJTs) in SiC have become popular because of their low on-state voltage drop, ease of manufacture, and high yields. Devices with blocking capability of 1.8 kV, 10 A [25] and 3.1 kV [26] have been demonstrated with good current gains. Although many difficult technological issues must be solved before viable ultra-high voltage SiC IGBTs can be commercialized, demonstration of 400 V, 2 A IGBTs operating at 400 °C [27] certainly show a promising start. Field controlled thyristors (FCTs) offer excellent performance and ease of manufacture [28] in SiC, but may require further refinements in materials and processing technology. Experimental demonstration of these 300 V, 1 A devices operating at 250 °C show the feasibility of this concept.

As a semiconductor material, SiC is projected to be far superior for the realization of devices capable of operating at high temperatures as compared to contemporary devices. This is because SiC has a high 'intrinsic temperature', defined as the temperature at which the intrinsic carrier concentration approaches the lowest doped region in the active power device. The intrinsic blocking voltage capability of a PN junction made with a particular material is lost at this temperature. For a voltage blocking layer doping of 10^{16} cm^{-3}, this temperature is 1320 °C for 4H-SiC, as compared to only 370 °C for silicon. Although many researchers have demonstrated SiC devices operating at temperatures beyond the conventional range of up to 150–175 °C, the reliable long term operation of these devices has not been proven. Some of these demonstrations in the past few years include: 100 V/1.2 A JFETs operating at 600 °C [29] for 30 h, 5 kV PiN diodes operating at 300 °C [4], MPS diodes operating at 250 °C [30], p-IGBTs operating at 400 °C [27], and 300 V Field controlled thyristors operating at 250 °C [28]. While devices that rely primarily on the characteristics of PN junctions like PiN diodes, BJTs and thyristors may not have physical limitations for high temperature operation, MOS-based and Schottky metal-based devices do face some fundamental physics-based issues as described above.

Despite these promising demonstrations by many groups around the world, there are some issues faced by SiC still preventing it as a material of choice for commercial power devices. Although some of these issues reflect the relative immaturity of this technology, some may require years of development, or may be fundamental to this new material system. As devices emerge that perform at temperatures exceeding theoretical limits of Si, new material and packaging reliability challenges will have to be addressed. The remainder of this paper will focus on physical performance and reliability issues for high power devices operating at slightly above the temperature range used for conventional Si device devices, i.e. 200–300 °C compared to a practical Si power device limit of 125 °C typical operating temperature.

2. SiC–dielectric performance and reliability

A natural oxide for SiC was considered a significant advantage for SiC as compared to other compound semiconductor materials since it enables the realization of the ideal switch in SiC, the power MOSFET for a wide variety of applications. However, some fundamental physics-based issues and technological development issues have prevented the realization of the full commercial potential of a MOS-based SiC power device, despite a decade long research on this device. A serious physics-based reliability challenge results from carrier tunneling into dielectrics. The most commonly cited intrinsic oxide degradation mechanism in SiC is the Fowler–Nordheim (FN) tunneling [31].

2.1. Fowler–Nordheim tunneling

Metal–dielectric–semiconductor-based devices under high electric fields can suffer from a serious long term reliability concern due to the Fowler–Nordheim (FN) tunneling current [31,32]. The electric field in the dielectric results in an emission of carriers from the semiconductor into the dielectric, or from the gate metal into the dielectric, resulting in time-dependent dielectric breakdown (TDDB). Such a breakdown occurs over a finite period of time (depending on the electric field, temperature, and the band offsets), and manifests itself with an increasing leakage current between the gate metal and the semiconductor. The tunneling emission current is of the form [32]:

$$J^0_{\mathrm{F-N}} = A \cdot E^2 \exp\left(-\frac{B}{E}\right)$$

where $J^0_{\mathrm{F-N}}$ is the tunneling emission current at zero temperature, E is the electric field in the dielectric, and A and B are dependent on the properties of the relevant

junction. The barrier height (Φ_B) is defined as the difference between the electron affinities of the metal/semiconductor and the dielectric. A and B have the following dependence on band offset:

$$A \propto \frac{1}{\Phi_B}$$

$$B \propto (\Phi_B)^{3/2}$$

Note that the tunneling current emission is *exponentially dependent* on both the electric field in the dielectric and the barrier height. The temperature dependence of FN tunneling is too complicated to be treated in this paper, and is treated in detail by Pananakakis et al. [32]. To the first order, the FN current can be assumed to be proportional to the square of temperature.

2.2. MOS in forward bias

Forward bias is defined to be when an NMOS device has a positive bias on the gate with respect to the source, or when a PMOS device has a negative bias with respect to the source. Most of the discussion here is concentrated on the NMOS case, while a similar parallel exists for the PMOS case. The barrier height for the purposes of FN tunneling is calculated as the difference between the conduction band of the dielectric and the Fermi level of the semiconductor. In the worst case scenario for an NMOSFET, the Fermi level may be assumed to lie at the conduction band edge, which corresponds to a very strong inversion case, or when highly doped N-type SiC is used. For this condition, the barrier height for FN tunneling is the conduction band offset (electron affinity difference) between SiC and the dielectric. The following discussion will assume SiO_2 as the dielectric. FN tunneling currents are expected to be much higher at a given temperature and electric field for SiC-based devices than for Si-based devices because the conduction band offset between SiC and SiO_2 is smaller than that between Si and SiO_2. As shown in Fig. 1, the conduction band offset in the Si–SiO_2 interface is 3.2 eV, but it is only 2.7 eV for 4H-SiC. For a similar FN tunneling current, this 0.5 eV difference in the band offset will require that the electric field in the dielectric for a 4H-SiC/SiO_2 system be reduced by approximately 1.5× as compared to a Si/SiO_2 system.

In commercial Si NMOSFETs, the electric field in SiO_2 is kept below 4–5 MV/cm, so that a reasonable 10 year life is achieved [33]. Tunneling is the primary device lifetime limiting factor for Si MOS-based devices, and is rated only to a maximum temperature of 125 °C. Reducing the electric field in the dielectric to 3 MV/cm for a SiC NMOS device will limit the maximum gate bias to only +15 V for the typical 50 nm gate dielectric thickness at room temperature. At higher temperatures, the electric field in the dielectric (and hence the gate bias) must be made even smaller in order for the SiC MOS reliability to approach that of a Si MOS transistor. Since the valence band offset of 3.05 eV is larger than the conduction band offset of 2.7 eV, PMOSFET reliability may be higher than NMOSFET reliability in the on-state of operation. Ironically, the wider bandgap of SiC seems like a liability rather than an asset for high temperature operation because its band structure occupies a larger portion of the SiO_2 band structure.

From this discussion, it seems that the gate tunneling current of a conventional SiC NMOS device is higher than Si NMOS devices at similar gate electric fields and temperatures. However, this conclusion is drawn from the worst-case scenario of assuming the barrier height for the purposes of FN tunneling is equal to the conduction band offset of 4H-SiC and SiO_2, i.e. the case of strong inversion. A significant gain in the barrier height may be achieved if the Fermi level in SiC is below the conduction band, i.e. an enhancement-mode MOSFET (with p-type SiC) under weak inversion condition [34]. The gate bias range when the MOSFET is under weak inversion conditions is determined by the doping of the p-type base region. At the onset of weak inversion, the barrier height (Φ_F) may be as much as 4.3 eV (1.6 eV + 2.7 eV, Φ_C), as can be see seen from Fig. 2. A barrier height of 4.3 eV will allow a higher temperature operation of 4H-SiC-based MOSFETs as compared to Si-based MOSFETs (with a maximum barrier height of 3.75 eV), for an identical on-state electric field in the dielectric. This assumes that channel mobilities for Si and 4H-SiC MOSFET are similar for an identical electric field in the dielectric. However, despite more than a decade of research, relatively modest success has been achieved in the realization of high channel mobilities [35] for enhancement-mode NMOSFETs. Because of the low channel mobility observed in most 4H-SiC-based MOS devices, a higher gate bias (and electric field) may be required in order to realize a low channel resistance in a SiC power MOSFET. This represents a challenge for achieving a high reliability in SiC-based MOS devices at all temperatures. Hence, there exists an on-state performance/gate dielectric reliability trade-off determined by the experimentally obtained channel mobility.

2.3. SiC–dielectric interface state density

The performance/reliability trade-off is severely influenced by traps and carrier energy states at the SiC–dielectric interface. The origin of these traps is linked to the imperfect nature of 4H-SiC/dielectric interfaces, due to the presence of carbon clusters [36] and/or dangling Si- and C-bonds. A significant number of electrons that are expected to provide the low on-resistance of the inversion layer get trapped in these energy states and scatter mobile electrons, further increasing the resistance in the channel region. Experimental data by Ouisse [37]

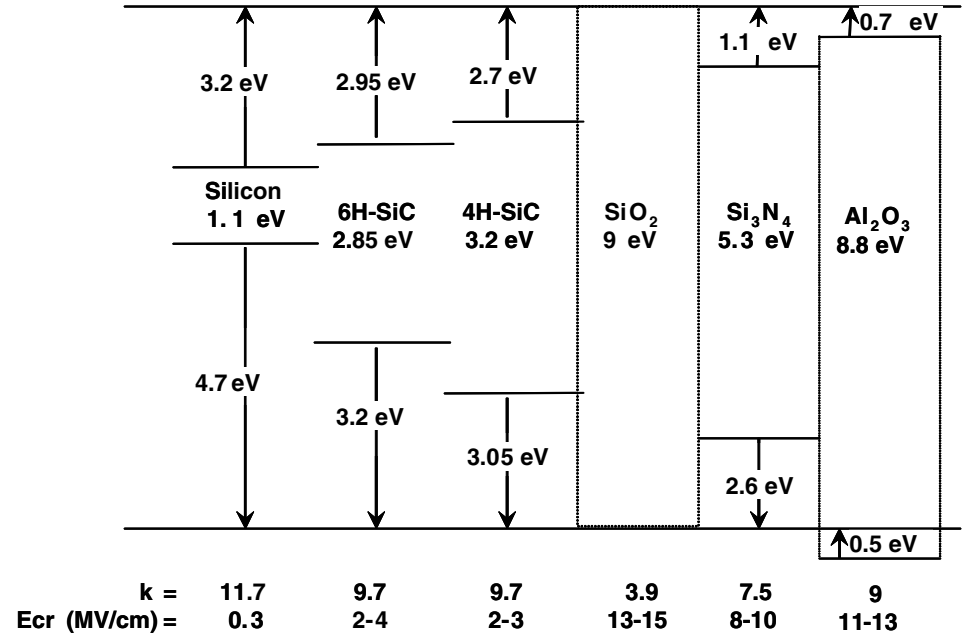

Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offests of these are also shown with respect to SiO_2.

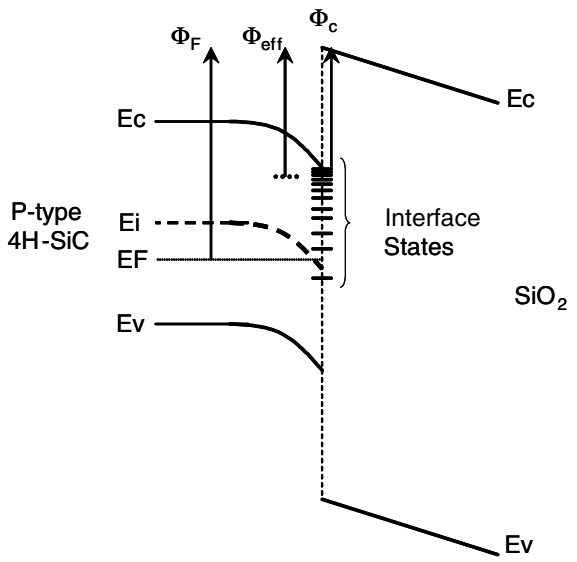

Fig. 2. SiC MOSFET under weak inversion case. The relevant barrier heights for FN tunneling in SiC–SiO_2 interface: Φ_C is the conduction band offset, Φ_F is the theoretical FN barrier height, and Φ_{eff} is the effective barrier height due to the presence of interface states at the SiC–SiO_2 interface.

shows that the low channel mobility in 4H-SiC is directly linked to extraordinarily high interface state densities in the SiO_2/SiC junctions. In the energy band diagram, the interface traps that influence channel mobility are located between the Fermi level and the conduction band of the SiC polytype used to make the MOSFET as shown in Fig. 2. Experimental data by Schorner [38] has shown that the density of these interface states in SiC exponentially increase beyond a level of 2.4 eV above the valence band of all SiC polytypes. In this study, the anomalously low electron inversion mobility in 4H-SiC MOSFETs (as compared to 3C, 6H and 15R SiC) was attributed to the largest bandgap of 4H-SiC among the commonly studied SiC polytypes.

The location and density of interface states within the bandgap influences not only channel mobility, but also the FN tunneling currents at the SiC–dielectric interface. The existence of a significant density of electrons at the interface states causes them to act as the primary source of FN tunneling current into the dielectric, rather than the position of the Fermi level [31]. Rather than a well defined barrier height determined by the difference between the Fermi level and conduction band, an 'effective' barrier height (Φ_{eff}) is typically observed in most cases which is determined by the density and location of the interface states [31] in the energy gap. Since most of the interface states are located close to the conduction band edge, Φ_{eff} is close to the conduction band offset of the SiC–SiO_2 interface. FN tunneling current data on n-type SiC by Li et al. [39] shows that the 'effective' barrier height is even lower than the 2.7 eV conduction band offset difference at room temperature, and it decreases to only 2.38 eV as the operating temperature is increased to 300 °C. Similarly, a lower FN tunneling barrier height

was experimentally observed in 4H-SiC PMOSFETs by Chanana et al. [40], indicating the strong influence of interface states on FN tunneling current rather than the position of Fermi level.

The low inversion layer mobility in power NMOSFETs may be acceptable for higher voltage (>2 kV) MOSFETs since a lower proportion of the resistance is contributed by the channel. However, if the MOS interface state density in these devices is high, their viability will be determined primarily by FN tunneling. The electric field in the dielectric must be kept correspondingly lower to limit FN tunneling current. The reduction in interface state densities in MOS structures will play a critical role in the on-state and high temperature performance, as well as reliability of power MOSFETs in 4H-SiC.

2.4. MOS in reverse bias

In addition to reliability challenges faced by 4H-SiC MOS devices in the on-state, they must be carefully designed in order to ensure good reliability in the reverse bias state. Consider an unterminated edge of a PiN diode with a lateral PiN region supporting the full blocking voltage, and a metal–oxide–SiC stack adjoining the PN junction, as shown in Fig. 3. For this diode to support the full voltage capability of SiC, the peak electric field at the PN junction is close to the critical electric field of SiC, which is approximately 2.5 MV/cm. According to Gauss' law, the electric field in the oxide is the inverse ratio of the dielectric constants, which are 9.7 and 3.9 for SiC and SiO_2, respectively. This implies that the electric field in the oxide is 6.2 MV/cm! Termination regions and other active regions in the devices must be designed carefully to prevent a high electric field at the SiC–SiO_2 interface.

Note that for reverse biased MOS, the bands bend in the opposite direction of that shown in Fig. 2, and the relevant barrier height for FN tunneling corresponds to the valence band offset, rather than conduction band offset. In contrast to forward biased MOS case, the electric field in the dielectric is determined by its dielectric constant and interface electric field, rather than thickness of the dielectric. The electric field in the oxide is not excessive in Si-based high voltage devices because the critical electric field of Si is about an order of magnitude lower than SiC. The high critical electric field strength of SiC can only be utilized to obtain high voltage SiC devices with SiO_2, which has the highest electric field strength of the commonly studied dielectrics, unless specific designs are adopted to alleviate the electric field in alternative dielectrics.

The issue of high electric fields in the dielectric is even more severe for power MOSFETs in SiC because it is generally more difficult to shield gate dielectrics from high electric fields. The three dominant families of Si and SiC power MOSFETs are: DMOSFETs, Trench-gate or UMOSFETs, and lateral MOSFETs. For lateral MOSFETs, the oxide breakdown location is similar to that shown in Fig. 3. For such MOSFETs [41], a high electric field exists at the p-base/drift region junction, resulting in a high electric field in the dielectric. In case of trench gate MOSFETs or UMOSFETs [42], an extremely high electric field exists in the oxide at the trench bottom [43], adjacent to the voltage blocking p-base/n drift junction, as shown in Fig. 4(a). The electric field

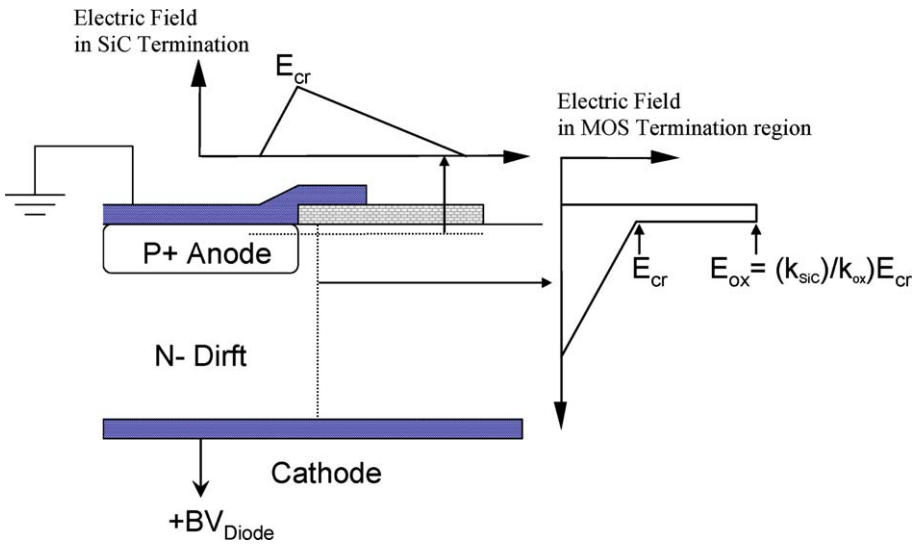

Fig. 3. Unterminated edge of a SiC PiN junction with a metal–oxide SiC stack beyond the PN junction. The electric fields in the SiC and the oxide–semiconductor interface are also shown.

concentration at the trench corners and the bottom is even more severe than the lateral case because the trench bottom must extend below the voltage blocking PN junction. A smaller pitch worsens rather than alleviate this problem because it will expose even larger area of the trench bottom oxide to high electric field. The electric field at the trench bottom may be lowered to some extent by placing deep p-type extensions below the p-base region [44], in a principle similar to a JBS diode.

The most promising structure for SiC power MOSFETs may be the DMOSFET structure shown in Fig. 4(b), from the standpoint of controlling the electric field in the gate oxide. The electric field at the SiC–SiO_2 interface is lowered by the electric field pinch-off effect from the adjacent p-base regions. This leads to a an acceptably low electric field in the gate oxide shown through simulations in [45]. However, this pinch-off increases the resistance of the DMOSFET by introducing a "JFET" region between adjacent p-base regions. The trade-off between the on-state resistance of the DMOSFET and the extent of reduction of electric field at the SiC–SiO_2 interface is determined by the spacing of the adjacent p-base region, as discussed in detail in [45]. During the evolution of Si DMOSFETs, the reduction in cell pitch resulted in a very high JFET region resistance. Hence, it was necessary to increase the n-type concentration of the JFET region through, for example, n-type ion implantation. For very high voltage SiC DMOSFETs (>2 kV), the lower doping of n-drift region will cause the JFET pinch-off to be severe, resulting in a high "JFET" region resistance. However, an n-type "JFET" implant in SiC DMOSFETs increases the electric field in the oxide to a higher level, as shown in Fig. 4(c). This trade-off is less critical for Si DMOSFETs because the electric field in the gate oxide for those devices is <1 MV/cm due to a lower critical electric field of Si.

2.5. Alternative dielectrics for higher reliability?

In contemporary deep submicron Si DRAM devices, alternative dielectrics are being studied [46] to enhance reliability, reduce on-resistance, and have a greater physical thickness versus electrical thickness for the dielectric. In order to alleviate some of the reliability concerns, dielectric materials other than SiO_2 have been explored for the SiC metal–dielectric–semiconductor (MDS) system [47]. Desirable properties for an alternative dielectric that may enhance the performance and reliability of an MDS structure are: (a) low interface state density; (b) high dielectric constant; (c) high dielectric breakdown strength; and (d) large conduction and valence band offsets.

For a reverse biased MDS structure, the electric field in the dielectric is inversely proportional to its dielectric constant, and FN tunneling current is exponentially dependent on the electric field in the dielectric. Therefore for an identical band offset, the FN current can be reduced dramatically if a dielectric with a slightly higher dielectric constant is utilized. A higher dielectric constant also reduces the inversion layer channel resistance since for a given voltage:

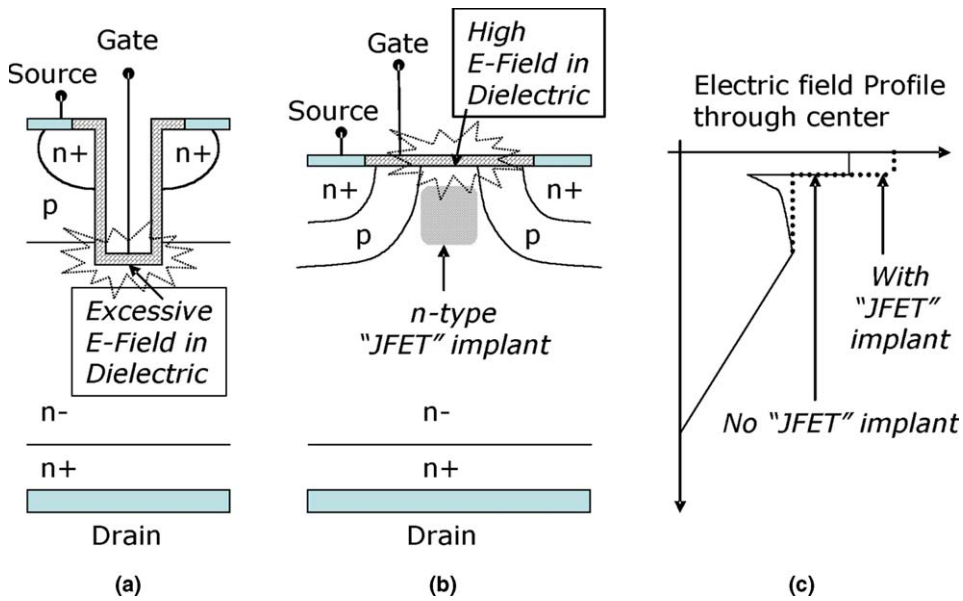

Fig. 4. High electric field location for (a) UMOSFETs and (b) DMOSFET power MOS structures. Electric field profile for a DMOSFET for the case with and without the JFET region implantation shown in (c).

$$R_{ch} \propto \frac{t_{diel}}{k_{diel}}$$

where R_{ch} is the resistance of the channel layer, k_{diel} is the dielectric constant, and t_{diel} is the thickness of the dielectric used to make the MDS channel. A detailed analysis of the impact of higher dielectric constant (high-k) on the on-resistance of SiC power MOSFETs is discussed in [43]. The reliability of MDS structures can be increased in the on-state if a thicker dielectric is used to reduce the on-state electric field, at the expense of the channel resistance. However, depending on the value of dielectric constant, the on-resistance may still be lower than for SiO_2. This allows more flexibility in the on-state performance/reliability trade-off. This is because, for a dielectric with larger k_{diel}, a thicker t_{diel} may be used for the same R_{ch}.

Although the electric field can be reduced if a high-k dielectric is used for a reverse biased MDS structure, it must still be lower than its breakdown electric field to prevent its rupture. Unfortunately, based on the analysis of a wide range of high-k semiconductor dielectrics like Si_3N_4, Al_2O_3, HfO_2, Ta_2O_5, ZrO_2, La_2O_3, Pr_2O_3, TiO_2, and $SrTiO_3$ [48], it has been found that the breakdown field strength decreases as their dielectric constant increases. Roughly, an empirical relation between E_{BD} and dielectric constatnt, k is of the form [48]

$$E_{BD} = 35k^{-0.64}\ \mathrm{MV/cm}$$

This may eliminate some dielectrics as possible replacements for SiO_2 for MDS structures.

What is even more disconcerting is the fact that conduction band offset of all these dielectrics with respect to 4H-SiC is smaller than that of SiC–SiO_2 [49], as shown in Fig. 5. *A direct replacement of SiO_2 with a high-k dielectric will not achieve a higher reliability because the primary limitation to reliability of SiC MDS devices is FN tunneling, which is strongly dependent on the conduction band offset between SiC and the dielectric*. Although Al_2O_3 offers very attractive properties, it is a difficult material from a device processing standpoint. Some high-k materials (like TiO_2 and Ta_2O_5) that were considered promising candidates for replacement of SiO_2 in the past [43,47] have negative conduction band offsets with respect to 4H-SiC! In general, the bandgap of dielectrics are inversely proportional to their dielectric constants [49]. This is the reason that most materials with higher-k will also have a smaller conduction and/or valence band offsets. Although little research has been done on the SiC–dielectric interface quality for any high-k dielectric, it may be many years before they can match the still modest quality of the SiC–SiO_2 interface. Hence, it is very unlikely that an alternative dielectric will replace SiO_2 as the dielectric of choice in SiC-based MDS structure.

One solution to exploit the potential for higher reliability and lower on-resistance of high-k dielectrics is to use a stack of dielectrics [45,46]. In this solution, a very thin (5–10 nm) high quality SiO_2 layer is in intimate contact with 4H-SiC, while most of the thickness of gate dielectric is composed of a high-k dielectric. During forward bias on this MDS structure, FN tunneling current can be lowered because a low electric field is achieved through the use of a much thicker high-k material for the same R_{ch}. As an example, if Si_3N_4 ($k = 7.5$) is used as the high-k dielectric in a SiO_2–Si_3N_4 stack, it can be made almost 2× thicker than a conventional pure-SiO_2 gate dielectric in order to achieve the same R_{ch}. While the conduction band offset is primarily determined by the SiO_2 layer, this 2× reduction in electric field will reduce the FN tunneling quite significantly. Of course,

	Dielectric Const	*Breakdown Fld (MV/cm)*	*4H-SiC Cond. Band Offset (eV)*
SiO_2	3.9	13-15	2.7
Si_3N_4	7.5	10	1.6
Al_2O_3	9	13.5	2.0
HfO_2	25	~6.7	0.7
TiO_2	26	~1.5	-0.4?
Ta_2O_5	95	~3	-0.4
$SrTiO_3$	200	~2.2	-0.9?

Fig. 5. Dielectric constant, breakdown electric field and conduction band offset with respect to 4H-SiC for commonly researched dielectrics.

the thickness of SiO_2 should be sufficient so that its conduction band offset, rather than that of the high-k dielectric determines the barrier height for the purposes of FN tunneling. The high-k dielectric should also be chosen so that its conduction band offset is not too small to influence the FN tunneling properties. The breakdown electric field, dielectric constant and the band offsets of two promising candidates for this stacked structure, Si_3N_4 and Al_2O_3, are given in Fig. 5. The stacked solution may not offer significantly improved reliability for a reverse biased MDS structure because the electric field in the thin oxide is still determined by the electric field at the SiC–SiO_2 interface, and its dielectric constant. However, with appropriate design, the electric field at the SiC–SiO_2 interface can be minimized to an acceptable level for most devices.

3. Schottky metal-based devices

While the reverse leakage current of PN junction-based devices in principle is largely determined by the bandgap of the semiconductor used, the reverse leakage current for Schottky junctions that are expected to block the rated voltage is dependent on the metal–semiconductor barrier height. In some of the most promising SiC-based power and microwave devices—the power Schottky diode and the microwave MESFET, a Schottky junction is required to block the rated voltage. To the first order, the leakage current in Schottky diodes is given by [34]

$$J_L = A^{**}T^2 \exp\left(-\frac{\Phi_{Bn}}{V_T}\right)$$

where A^{**} is the modified Richardson constant, T is the operating temperature, Φ_{Bn} is the metal–semiconductor barrier height, and V_T is the thermal voltage. This equation shows that the leakage current in a voltage-blocking Schottky junction is exponentially dependent on the metal–semiconductor barrier height and the operating temperature. Since SiC power Schottky diodes are expected to compete with Si PiN diodes, they must have a comparable forward on-state voltage drop. The most commonly used Schottky metals (e.g. titanium and nickel) have Φ_{Bn} values close to Si bandgap value of 1.1 eV [50]. The high temperature blocking performance of these Schottky diodes will only approach that on Si PiN diodes, which is in the 125–175 °C range, and not the 250–350 °C range promised for many PN junction-based devices. The metal–Schottky barrier height is further reduced due to the effect of barrier height lowering when a high reverse electric field is present at the metal–SiC interface during blocking [50]. The presence of material defects also increases the leakage current in SiC Schottky diodes because these defects act as sites with lower Schottky barrier heights as compared to the bulk of the device [61]. Since the leakage current is exponentially dependent on the Schottky barrier height, even small areas with low Schottky barrier heights will contribute a significant portion of the leakage current, and will be even more severely influenced by increasing temperature than if a uniform Schottky contacts is assumed [61].

For microwave MESFETs, the limitation of choosing a low barrier height metal is not as severe because the Schottky contact is in the blocking mode. However, a survey of metal–semiconductor barrier heights in SiC [51] shows that most commonly used metals have Schottky barrier heights in the 1.0–1.9 eV range. Even if the highest barrier height metal is chosen to form the SiC MESFET, the high temperature performance of these devices may not achieve the high temperature promise of SiC devices. Schottky contacts in MESFETs are present in channel regions where much higher temperatures are observed as compared to the bulk of the device. This temperature differential can exceed 75 °C [52] because current densities in the MESFET channel regions can exceed 10^5 A/cm^2! Since gate metal width has to be minimized for high frequency MESFETs, the choice of Schottky metal for its formation is limited by the fabrication procedures used. It is sometimes difficult to choose a large Schottky barrier height metal like platinum and gold because of such limitations. These issues will limit the operating temperature of SiC Schottky-based devices to silicon-like levels.

4. Materials defect impact on performance and reliability

It is well known that SiC occurs in many polytypes in nature, with different bandgaps, carrier mobilities, and crystal structures. The most commercially relevant polytypes for the manufacture of power devices are 4H-SiC and 6H-SiC [53]. These polytypes offer high breakdown electric fields ($>2\times10^6$ V/cm), high carrier mobilities, and relative maturity in wafer quality. Presently, these wafers are commercially available in 3 in (75 mm) diameter size with device-grade crystal quality. Larger wafer sizes are necessary to reduce the device cost and enable the widespread adoption of SiC power devices, as exemplified by other semiconductor technologies.

4.1. Material defects in SiC

The most prominent defect in SiC is the micropipe, and many commercial wafers are graded according to this specification. A micropipe is a thermodynamically stable hollow core screw dislocation [53], which shows as a hole through a wafer within a ±15° off the c-axis of the wafer and is close to 1 μm diameter in size. It has been shown that a SiC device with a micropipe in its active area cannot support significant electric field

[54], and hence any significant power level. The micropipe densities in commercial wafers are steadily decreasing as material growth techniques mature, and presently it is possible to purchase wafers with a micropipe density of 5–10 cm^{-2}. However, it is imperative that this 'killer defect' be eliminated in the future for the realization of high current power devices.

Besides micropipes, there are many material defects commonly observed in present-day SiC. These defects can be broadly classified into wafer-level defects and epitaxial defects. Usually SiC wafer defects act as nucleating sites for epitaxial defects that may affect device performance. Various defects on bare SiC wafers are:

1. Closed core screw dislocation (with a typical 1000–5000 cm^{-2} density) is an ordered crystal defect, similar to a micropipe, that runs continuously over significant thickness of wafer. Depending on the epitaxial growth method, it may continue to grow into the epitaxial layers. If an active voltage blocking junction is formed on such a defect, a ~20% reduction in critical electric field can be observed [55]. These defects may result in a reduction in carrier lifetime of epitaxial layers grown over them [56].
2. Basal plane dislocations (typical density: 10^2–10^5 cm^{-2}) are islands of single crystal SiC with a displaced basal plane which may be annealed using advanced epitaxial growth techniques [57].
3. Edge dislocations (10^4–10^5 cm^{-2}) are usually one-dimensional defects on the surface of wafers that get annealed during the epitaxial growth, and rarely affect properly designed devices.
4. Low angle boundaries (10^2–10^3 cm^{-2}) and polishing damage found in commercial wafers result in increased leakage currents during reverse bias operation of the these devices.

Defects in SiC epitaxial layers depend on the methods and reactors used to grow the layers. The most common epitaxial defects are growth pits (1–100 cm^{-2}), triangular inclusions of different polytype (e.g. 3C in 4H), carrot (0.1–10 cm^{-2}) and comet tail defects [58]. Growth pits and carrot defects result from wafer defects that create adverse conditions for the realization of a perfect crystal structure during epitaxial growth. Temperature non-uniformities during epitaxial growth cause the appearance of triangle inclusions of different polytypes. Poor management of impurities or premature nucleations of SiC particulates cause the formation of comet tails and other defects.

4.2. Reverse characteristics of SiC devices

When devices are in the reverse blocking mode, i.e. reverse biased Schottky and PN junctions, devices are expected to have low leakage current and have near-theoretical blocking voltage. From a reliability perspective, it is important to understand the affect of materials and processing defects on leakage current, total blocking voltage achieved, and sustainable avalanche energy achievable during breakdown. The effect of material defects on the device blocking performance has been discussed extensively by Neudeck et al. [56], Kimoto et al. [58] and Lendenmann et al. [59]. The most extensively studied defect in SiC is the screw dislocation [60]. Screw dislocations in PN diodes result in a higher leakage current, a softer breakdown I–V characteristics, and cause the breakdown microplasma to concentrate through this defect. Although the leakage current mechanism is dominated by this defect, measurements over a 298—673 K temperature range show that the leakage current is tolerable in diodes with screw dislocations. The leakage current near avalanche breakdown voltage is similar in diodes with and without screw dislocations. In fact, a peak avalanche power density of 140 kW/cm^2 was applied in diodes with screw dislocations with repeatable reverse I–V characteristics. This indicates that a screw dislocation does not cause severe reduction in blocking voltage of power devices fabricated on them.

Schottky devices (e.g. power Schottky diodes and MESFETs) are very sensitive to surface and morphological defects. Even small areas with material defects that cause reduced metal–semiconductor barrier height, can dominate reverse blocking characteristics [61]. This is because leakage currents in Schottky contacts are exponentially dependent on barrier height. Epitaxial growth, which is the main cause of morphological defects, is a much more important process for reliable and high yielding Schottky devices as compared to PN diodes. However, triangular 3C inclusions are quite devastating for blocking properties of both PN and Schottky devices. They result in >50% reduction in blocking voltage [56]. Carrots and comet tails result in some increase in leakage currents, but do not cause a severe reduction in blocking voltage. Small growth pits seem to affect Schottky diode more severely than PN junction devices [56]. With the improvement of epitaxial processing these affects may be minimized for most SiC power devices.

4.2.1. Avalanche energy

The pulsed avalanche energy is the amount of energy that the power device can handle safely while it is undergoing avalanche breakdown. This energy is determined by the adiabatic heating of the blocking layer and the intrinsic temperature of this low doped SiC layer. The static avalanche power density of a PN junction made using a particular material depends on its density, specific heat, and the temperature at which the intrinsic carrier density becomes close to the doping density of the voltage blocking layers (i.e. the bandgap of the mate-

rial). Theoretically, the total avalanche energy is calculated to be more than 10× higher than Si devices [62]. However, the breakdown current can become dominant over small filaments where all the breakdown microplasma is concentrated. This is true for both Si and SiC devices, and usually, material defects in voltage blocking junctions initiate these microplasmas. Experimental results on SiC PN diodes fabricated show that approximately 5× higher avalanche energy was obtained as compared to Si PN devices in steady state.

4.2.2. Blocking stability demonstrations

Early indications of biasing SiC PN junction devices to their avalanche breakdown limits indicated that SiC devices may have a negative temperature coefficient of avalanche breakdown value [62]. However, later experimental results conclusively disproved these early observations [63]. Although the cause of the observed negative coefficient of avalanche breakdown was never conclusively determined, a hypothesis pointed to the role of crystal defects in this phenomenon. It is possible that poor process fabrication conditions used resulted in surface contamination or surface states, which led to these unstable blocking characteristics of SiC diodes.

With rapid introduction of commercial power devices, close attention is being paid to reliability of power devices under all conditions. The material defects like micropipes are primary yield limiting factor for these devices. The first reported reliability testing on SiC Schotttky diodes were made in 1999 by Rupp et al. [64]. In this study, 100 devices with 600 V rating were tested for (a) thermal cycling up to 400 °C; (b) cycling between −55 °C and 150 °C for 1000 times; (c) high temperature reverse bias at 150 °C with a reverse bias of 600 V for 1000 h; and (d) high humidity, high temperature reverse bias testing (85 °C, 85% relative humidity) for 1000 h. None of these tests resulted in any failures. Yield on 600 V, 6 A Schottky diodes exceeded 75% in this report. Recently, another group [65] has also shown a total of 145,000 device-hours of high temperature reverse bias testing, 11,000 device-hours of continuous current "burn-in" testing, and 35,000 device-hours of power cycling testing with no failures.

In a statistically significant study, higher voltage (3.2–4.0 kV) packaged PiN diodes were biased at 2250 V under high temperatures (125 °C) for 500 h [55] without showing catastrophic failure. In these devices, the leakage current remained in the 10^{-8}–10^{-4} A/cm^2 range. It is worthwhile to note that in this study, many devices had a widely varying (factor of 10^4) level of leakage currents, but remained stable with time and temperature. Although a few diodes showed sporadic increases in leakage currents, the total leakage current remained below 10^{-4} A/cm^2 range. Many of these variations in leakage currents and their sporadic increases were probably caused by material and processing defects/variations.

These demonstrations have proven that although materials defects may cause limitations to yield and device performance in the blocking state, they do not result in severe long term issues with respect to their blocking reliability and stability. These observed experiments are true for both PN and Schottky junction devices.

4.3. Forward voltage degradation in SiC PN diodes

While the reverse bias operation of SiC devices have been found to be relatively stable, a curious phenomenon observed recently during the forward bias operation of SiC PiN diodes has caused a great deal of concern towards long term stability of these devices. It has been observed that as PN diodes are forward biased for an appreciable length of time, their on-state voltage drop increased with time, as shown in Fig. 6. The duration over which these devices show this forward bias degradation varies from a few milliseconds to many hours [66]. A variation in on-state voltage drop (V_F) in PiN diodes has serious stability concerns because it can result in current filamentation and local current 'hogging'. If a portion of the diode has a lower on-state voltage drop than another region within the same diode due to slight differences in material and processing variations, current will be diverted into the lower V_F region. This can cause excessive current densities in small portions of the diode, while leaving large portions of it with a low current density, leading to thermal instability of the entire diode. Such characteristics will also prevent safe paralleling of devices to boost the total current required for typical

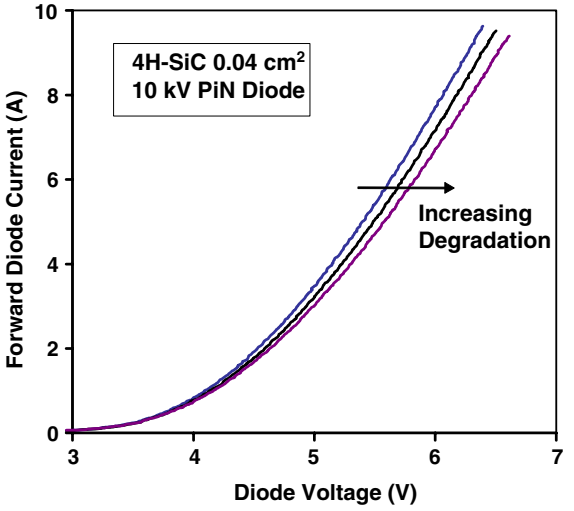

Fig. 6. On-state characteristics of a high voltage SiC PiN diodes after various levels of forward bias stress.

high current applications for which these devices are targeted.

4.3.1. The observed phenomenon

Optical observation of PN diodes undergoing V_F degradation shows a concomitant formation of a certain material defect in these diodes, as shown in Fig. 7. Probably the first report of this phenomenon, which were termed as 'Bright line defects' since they appear are mobile bright lines, was made by Konstantinov et al. [67]. This was compared to the previously studied formation of 'Dark line defects' in gallium arsenide light emitting devices [68], where dislocation growth due to non-equilibrium carrier injection and crystal strain results in a similar forward bias degradation phenomenon. Many researchers agree that mobile and propagating crystal stacking faults are the primary cause of forward bias degradation of PN diodes. This defect propagates through the entire n-base layer. It was initially proposed [69] that the increase in V_F is caused by reduced carrier lifetimes due to the formation of recombination centers from stacking faults. However, more recent results indicate that the increase in V_F occurs as the stacking faults form a barrier to current flow and reduce the conduction area. A stacking fault defect is usually a two-dimensional error in the atomic stacking sequence of a polytype of SiC.

Fig. 8 shows a series of light emission images at various intervals during degradation for two adjacent 0.015 cm^2 diodes on the same chip. These optical phenomena were correlated with a lifetime measurement method that uses the turn-off reverse-recovery waveforms for conditions of high dI/dt and low dV/dt [71]. The result of this study indicates that the effective base lifetime is not reduced and the V_F degradation is due to a reduction in conduction area. Fig. 9(a) and (b) show the forward bias voltage degradation and reverse recovery current for the same diodes as those shown in Figs. 7 and 8, where the arrows on Fig. 9(a) and (b) indicate the time for each frame in Fig. 8(a) and (b), respectively. The rhomboid shaped regions in Fig. 8(a) indicate stacking faults emanating from near the surface, presumably from the P–N junction. These stacking faults are near the surface by the growth direction and shape as well as the focal plane of the CCD camera. The device degrades rapidly in Fig. 9(a) because the highest excess carrier concentration is near the P–N junction. The outlined triangular dark regions in Fig. 8(b) indicate stacking faults growing from near the bottom of the drift region. The white outlines are from partial dislocations that bound the stacking faults and the dark regions indicate regions where current is reduced. The device degrades more slowly at first, as can be seen in Fig. 9(b), because the stacking faults are near the bottom of the drift layer where the excess carrier concentration is lower and the degradation rate increases as the stacking faults approach the P–N junction at the surface where the excess carrier concentration is larger.

The fundamental nature, origin and propagation of these dislocations have been extensively investigated by various researchers [69,70,72]. These defects nucleate from existing substrate crystal defects in hexagonal (e.g. 4H and 6H) SiC. The hexagonal crystal structures of these polytypes of SiC are formed when three distinct atomic patterns are stacked in a particular sequence. This is in contrast with cubic (3C) SiC, which has a fundamentally two-dimensional structure with only two atomic patterns stacked together. Hence, 4H-SiC and 6H-SiC crystals are metastable at room temperature and could convert to a locally faulted 3C-like structure

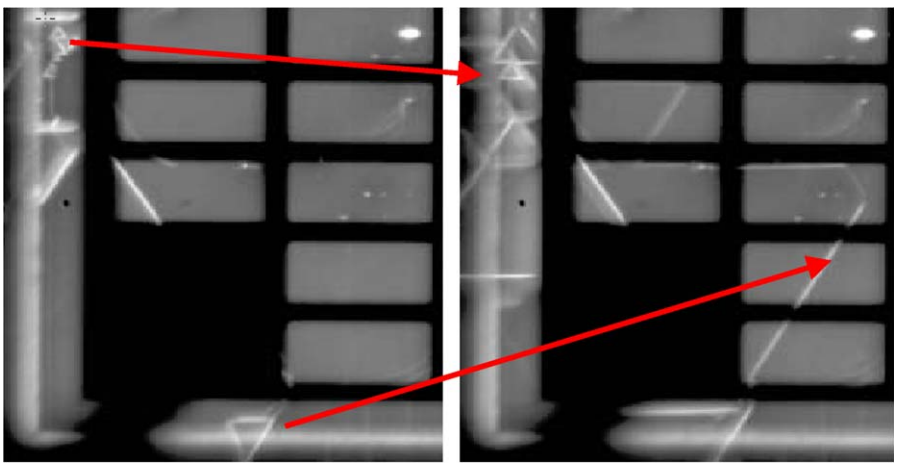

Fig. 7. Light emission measurements of a PiN diode before (left) and after (right) forward bias stress indicating growth of stacking faults.

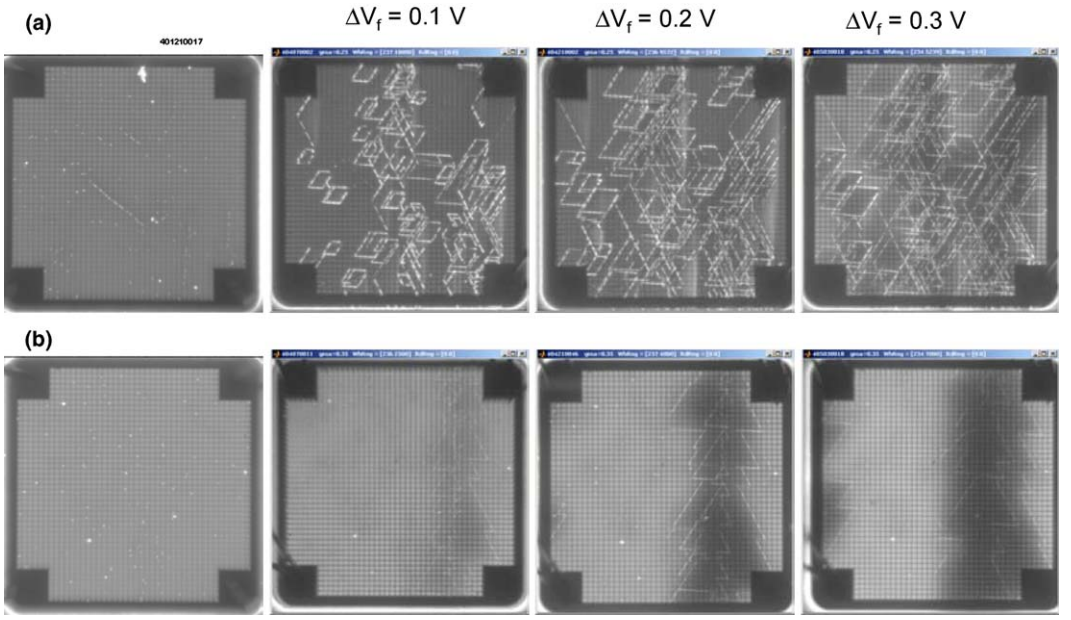

Fig. 8. Light emission images at various intervals during degradation for two adjacent diodes (a) top and (b) bottom on the same chip.

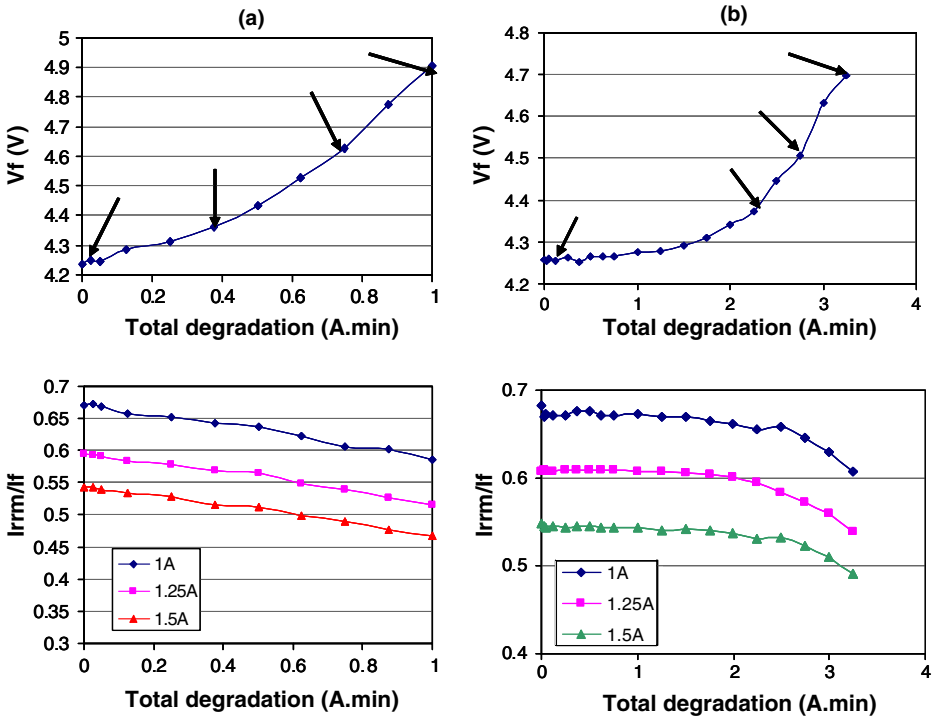

Fig. 9. The on-state voltage V_F (at 100 A/cm^2) degradation and reverse recovery current for the same diodes in Fig. 8(a) and (b), respectively.

if an appropriate nucleating site was present [73]. For this to occur, a proper type and density of nucleation sites and the activation energy in the form of electron–hole pair recombination are needed. The control of the

origin and propagation of these defects may lie in the control of pre-existing defects serving as nucleation sites for these defects.

The incidence of propagation of these dislocations was found to increase with higher current densities [66,73,75]. Higher temperatures and thicker epitaxial thicknesses also resulted in a higher incidence of formation of dislocations. Probe scratches [75], chip scribe lines and even silicided contacts on PN diodes are considered to be nucleation sites for mobile and expanding dislocations [74].

4.3.2. Electroluminescence studies and activation energy of fault generation

Electroluminescence analysis of the emission spectra found that bright line defects emit light in the red and near-infrared spectral regions, in contrast to near-band-gap luminescence of non-degraded PN diodes which is predominantly in the violet region [70]. These defects were determined to be an irreversible formation of a network of linear defects related to crystal dislocations that subsequently propagate through, and then beyond the diode area. The nucleating sites for these stacking faults appear to be primarily at low angle grain boundaries, among other substrate and surface defects. The resulting stacking faults have been observed to be bound by Schockley partial dislocations with a Burger's vector $b = 1/3\langle 1\,0\,-1\,0\rangle$[72]. This implies that the faults propagate as triangular or rhombohedral structures with edges along the 11–20 directions. These looping structures multiply and propagate as the diode is kept in the forward bias state. Spectral measurements show that the stacking faults have a primary emission spectrum in the 450 ± 20 nm peak range [70], and those of threading dislocations is in the 700 ± 20 nm range. The calculated activation energy for the gliding (propagation) of the partial dislocation that bounds the stacking fault is measured to be in the 0.27 ± 0.02 eV range. The estimated velocity of propagation of these defects was 7×10^{-5} m/s.

4.3.3. Solutions for V_F degradation problem

An activation energy of 0.27 eV is small enough that most nucleating sites will result in the formation of these faults, and hence some degradation in the on-state voltage drop of PiN diodes. Hence, the solution for solving this problem lies in minimizing the defects in the active portion of the device. A novel approach to achieving this was recently demonstrated by growing Lely crystals with no micropipes and only minimal defects on top of standard substrates [74]. In this experiment, an application of 200 A/cm^2 stress in the forward direction did not produce any degradation, which was observed with pn junction diodes using normal substrates. Recently, great strides have been made in 4H-SiC epitaxy to produce PiN structures with relatively stable characteristics by reducing the material defect density [76]. From these preliminary results, it seems that reduction of material defects would be directly correlated to obtaining a high yield of drift-free PiN diodes in SiC.

Also, various other methods have been investigated for improving the V_F degradation [77]. The different methods produce different yields of degradation-free devices with some processes having yields as high as 86% degradation-free devices. In each degradation-free process, some devices do not drift at all, while others drift a small amount and then stabilize. However, some of the processes also reduce the breakdown voltage yield. Most recently, a new low basal plane dislocation (BPD) process demonstrates substantial increase in the overall yield with blocking and drift yields of 35% and

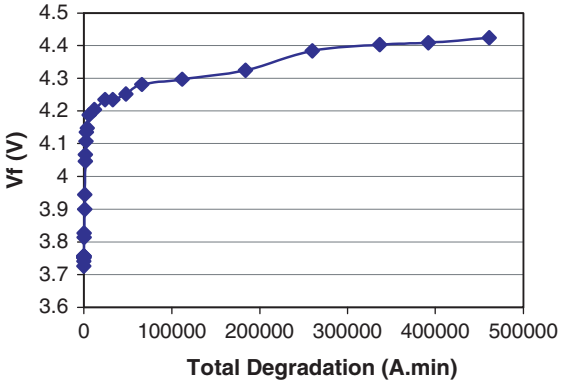

Fig. 10. On-voltage V_F (at 50 A/cm^2) degradation as a function of total degradation for a 0.5 cm^2, 10 kV 4H-SiC PiN diode stressed at 50 A.

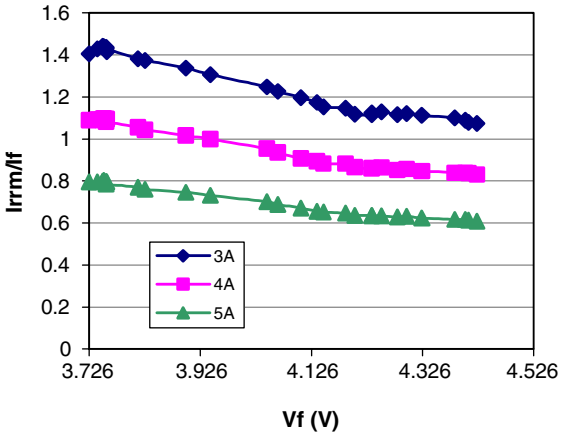

Fig. 11. Correlation between the reverse recovery peak as a function of total degradation for a 0.5 cm^2, 10 kV 4H-SiC PiN diode.

67%, respectively [78]. Figs. 10 and 11 show the degradation and monitoring results for a typical low degradation rate 50 A, 10 kV 4H-SiC PiN diode made with this process.

It is worthwhile to note that such a phenomenon is *not* observed in unipolar devices like Schottky diodes, even when the power density (on-current $\times V_F$) approaches near levels at which the PN diodes show this phenomenon [55]. While detailed published reports are missing, anecdotal data suggests that the forward bias degradation associated with dislocations occurs in bipolar SiC devices like thyristors, GTOs, PiN diodes, and even bipolar junction transistors (BJTs), but is not observed in unipolar switches like MOSFETs and JFETs.

5. Conclusions

Despite the remarkable results demonstrated by many groups around the world in exploiting the superior properties of SiC for high power and high temperature devices, there are reliability issues faced by SiC as a material of choice for commercial power devices. Although some of these issues reflect the relative immaturity of this technology requiring years of development, some may be fundamental to this material. A natural oxide–SiO_2, is considered a significant advantage for realizing a power MOSFET in SiC, which has great commercial potential. However, the performance/reliability trade-off for these devices is more severe than Si power MOSFETs because of the substantially lower MOS channel mobilities, smaller barrier height to tunneling, and higher experimentally obtained interface state densities. An approach investigated in this paper is the use of alternative dielectrics with higher dielectric constants, which may reduce the electric field in SiC MOS devices. However, many of these materials suffer from correspondingly lower breakdown field strength. High breakdown electric field strength of SiC also affects the choice of passivating dielectrics used in the edge termination and active regions of power devices.

Since the electric fields in dielectrics scale inversely with their dielectric constants, SiO_2 sees a 10× higher electric field during reverse bias operation of these devices, as compared to Si devices. This problem is further exacerbated in trench-gate MOSFETs because of field crowding at trench corners. This is another motivation for exploring high dielectric constant-high dielectric strength materials for SiC power devices. The higher bandgap of SiC has often been cited as a reason for pursuing high temperature power devices because of their correspondingly lower leakage currents. However, the reverse leakage currents in Schottky-based devices are dominated by the Schottky barrier height of these materials. Since the barrier height of commonly used Schottky metals for SiC devices is in the 0.7–1.2 eV range, the temperature performance of these devices will be similar to Si PN junction-based devices. This problem gets very severe in power MESFETs because the gate regions routinely see a much higher local temperature, as compared to the device ambient temperatures.

Material defects in present day SiC are the cause of many technological challenges faced by SiC devices. Wafer-level defects include micropipes, closed-core screw dislocations, basal plane dislocations and low angle grain boundaries. In the active device regions (epitaxial layers), some of these defects may be annealed if good epitaxial techniques are employed, but others result in (a) reduced critical electric field in devices; (b) higher leakage currents during reverse bias operation; and (c) degradation in the on-state performance of bipolar devices. Although many of these defects affect the reverse characteristics of high voltage SiC devices, long term operation of many devices have revealed that optimally processed devices do not suffer from reliability issues. This has allowed for the commercialization of the power SiC Schottky diode. Although the avalanche energy of SiC power devices is experimentally determined to be 3–10× higher than conventional Si power devices material defects have been shown to cause filaments that concentrate the plasma of the avalanche current. Detailed experiments conducted recently on bipolar SiC devices have shown that the on-state voltage drop in such devices increases with time when they are kept in the forward biased mode for appreciable length of time. Optical observation of PN diodes undergoing V_F degradation shows a simultaneous formation of mobile and propagating crystal stacking faults, that are responsible for a reduction in the diode conduction area.

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