A 10-kV Large-Area 4H-SiC Power DMOSFET With Stable Subthreshold Behavior Independent of Temperature

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***Abstract*—This paper presents the development and demonstration of large-area 10-kV 4H-SiC DMOSFETs that maintain a classically stable low-leakage normally off subthreshold characteristic when operated at ≤ 200 °C. This is achieved by an additional growth (epitaxial regrowth) of a thin epitaxial layer on top of already implanted p-well regions in conjunction with a N_2O-based gate oxidation process. Additionally, the design space of the DMOSFET structure was explored using analytical and numerical modeling together with experimental verification. The resulting 0.15-cm^2 active 0.43-cm^2 die DMOSFET with 10-kV breakdown provides $I_{DS} = 8$ A at a gate field of 3 MV/cm, along with a subthreshold current at $V_{GS} = 0$ V that decreases from 1 μA (6.7 μA/cm^2) at 25 °C to 0.4 μA (2.7 μA/cm^2) at 200 °C.**

***Index Terms*—Power MOSFETs, power switching, silicon carbide, subthreshold behavior.**

I. Introduction

OF GREAT interest for high-voltage (10+ kV) switching applications is the 4H-SiC DMOSFET because it combines the high-breakdown low specific on-resistance of the 4H-SiC drift region with the majority carrier operation of the MOSFET, thereby accruing both low switching losses and the uniform current distribution needed for device paralleling. These attributes have made the 4H-SiC DMOSFET attractive as a potential candidate for insertion into future 10+ kV power switching architectures [1]. The lower switching losses of the SiC DMOSFET allow the architectures to be designed around higher frequencies ($\geq$ 20 kHz), substantially reducing the overall system size and weight of solid-state power switching applications.

Significant effort has been made in the development of 4H-SiC DMOSFETs, primarily in the 1+-kV range, including work on optimizing the design of the DMOSFET structure [2]. However, because of their thinner drift layers and low specific on-resistances, these lower voltage SiC DMOSFETs are smaller in area and have different equivalent circuit design considerations than used with 10-kV SiC DMOSFETs. The 10-kV SiC DMOSFETs have recently been scaled up in current output, with die sizes increasing from 0.11 cm^2 (0.0476-cm^2 active area) to 0.3 cm^2 (0.15-cm^2 active area) reported, capable of 5–10 A at room temperature [3], [4]. In addition to these useful improvements in blocking voltage and ON-state current, it is essential that DMOSFETs demonstrate a stable subthreshold characteristic over the projected operating temperature range (≤ 200 °C). This is critical in order to satisfy the need for both a normally off device and a device with an OFF-state leakage that does not compromise its blocking voltage at higher temperatures. The large-area SiC DMOSFETs reported in the literature, which have provided their subthreshold behavior as a function of temperature, have tended to become normally on or have excessive OFF-state leakage when operated at high (> 150 °C) temperatures due to an apparent temperature-dependent fixed charge voltage shift in their subthreshold characteristic [5].

In order to create a viable 10+-kV SiC MOSFET, a robust process is required that achieves a sustainable yield of large-area devices that have low-leakage normally off subthreshold characteristics above 150 °C. In this paper, we report on the successful development and demonstration of such a large-area 10+-kV SiC MOSFET process.

II. Design Considerations

The fabrication of 4H-SiC DMOSFETs in the 10+-kV range poses particular challenges resulting from the limitations of currently available SiC material quality and the required thick ($\sim$100 μm) drift region to achieve 10+ kV, competing with the need for large-area devices. As the power switching modules that would use these 10-kV devices are specified to carry over a hundred amperes, even paralleling several DMOSFET parts in each module still requires each DMOSFET die to have a large active area in addition to a large area devoted to junction termination extension (JTE) that allows 10+-kV breakdown. For example, at room temperature, a 100-μm drift region doped at 5×10^{14} cm^{-3} that is appropriate for 10-kV blocking will have a specific on-resistance of 133 m$\Omega \cdot$ cm^2. Thus, considering the drift resistance alone, a 10-A part in a package capable of removing 750 W/cm^2 of waste heat from the part would

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require at least an active area of 0.133 cm^2, and when the effects of self-heating at elevated power levels are considered, an even larger active area would be required to maintain the 10-A current level and thereby compensate for the increased drift resistance associated with the inverse relationship between carrier mobility and temperature. However, using 0.133-cm^2 active area as a baseline and if the active area is a square with a lateral JTE length of 500 μm, the final die size would then be 0.216 cm^2. Large die areas such as this suffer from a pronounced sensitivity to the defect density in the 4H-SiC material, creating substantial challenges in developing robust processes that have useful yields of 10-kV devices. This has been previously illustrated even at the 1-kV level, as 1200-V 4H-SiC vertical JFETs have been reported to have a decrease in their observed breakdown voltage with respect to the theoretical maximum allowed by the drift conditions, from 93% for VJFETs with 1.23×10^{-3}-cm^2 active areas to 91% for 0.068-cm^2 active areas [6], [7].

These problems are in addition to the requirement that 4H-SiC MOSFETs maintain normally off behavior as a function of temperature. If, as has been observed [5], the subthreshold behavior shifts toward a normally ON-state as a function of increasing operating temperature, even if the device remains normally off (i.e., a positive threshold voltage), the increase in OFF-state leakage associated with the shifting subthreshold region can dramatically reduce the breakdown voltage of the device independent of the JTE design.

In order to ameliorate these issues, a successful large-area 10+-kV MOSFET is required to employ a higher degree of margin in the design rules and process techniques than used for lower voltage material. An example of this is in the choice of drift thickness and doping. Assuming the adoption of a punchthrough structure, a theoretical 10-kV breakdown could be achieved with a 75-μm-thick drift doped at 9×10^{14} cm^{-3}, with a specific on-resistance of only 57 $m\Omega \cdot cm^2$, which is less than half the specific on-resistance of drifts actually used in 10-kV devices. The reason for the difference is twofold: 1) The defects inherent in the material reduce the achievable breakdown voltage of the device, a problem exacerbated for larger devices which contain more defects, and 2) variations in thickness and doping of epitaxially grown films necessitate conservative specifications for these films in order to ensure that the resulting drift layer will be capable of blocking the desired voltage.

Fig. 1 shows an analytical model of the breakdown for a 4H-SiC punchthrough drift structure as a function of thickness and doping level. Given the presence of defects and limitations on JTE design due to process variance, an at least 25% margin above the 10-kV range is desirable to maximize the likelihood of achieving 10-kV MOSFETs with reasonable yield. Additionally, the epitaxial vendor was only able to specify doping within $\pm 25\%$ and thickness within $\pm 10\%$ for this region of thick, low doped drift. Thus, Fig. 1 highlights the resulting region for a nominally 100-μm layer doped at 5×10^{14} cm^{-3}, becoming 90–110 μm and $3.75 \times 10^{14} - 6.25 \times 10^{14}$ cm^{-3} based on these error bars, respectively, and shows that the minimum breakdown for this process space is 12.5 kV, incorporating the desired 25% margin above 10 kV.

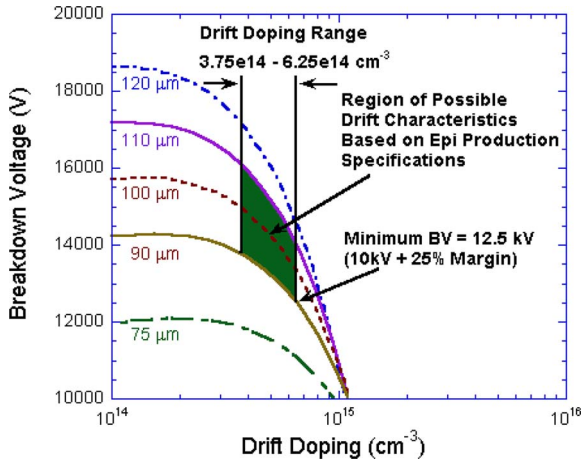

Fig. 1. Analytical model of breakdown voltage for a SiC punchthrough drift region nominally doped at 45×10^{14} cm^{-3} ($\pm 25\%$) and 100 μm ($\pm 10\%$) thick, appropriate for 10-kV operation with a 25% margin.

Having defined an appropriate drift region thickness and doping to meet the OFF-state blocking, the ON-state properties still require optimization, involving both the MOS channel characteristics (mobility, threshold voltage, etc.) and the physical layout of the device. Unlike 1+-kV SiC DMOSFETs which are very sensitive to channel resistance and channel mobility, the higher resistance of the drift in 10-kV DMOSFETs makes the channel resistance and mobility much less of a contributor to the total device on-resistance. DMOSFETs of 10 kV do, however, share a common sensitivity to threshold voltage and subthreshold stability as a function of temperature. It has been observed, however, that SiC MOS channels of higher mobility and lower resistance, which are formed using an NO oxidation method, have low and even normally on threshold voltages, as well as subthreshold characteristics that shift toward a leaky state as temperature increases [5]. For this reason, a twofold approach to stabilizing the threshold voltage as a function of temperature was taken. First, the channel performance was improved using an epitaxial regrowth (performed at Northrop Grumman Corporation) above the implanted p-well region in conjunction with a N_2O gate oxidation process. The use of a similar epitaxial regrowth layer above the implanted p-well has previously been shown to improve the channel resistance [8], [9] and, in this paper, is shown to also improve the subthreshold/temperature characteristics. The second aspect was to design and fabricate an array of small-area DMOSFETs in order to pragmatically explore the device geometry design space.

III. Experimental Determination of Channel Process and Device Geometries

Efforts to explore the 10-kV DMOSFET geometry design space and the channel process were performed in parallel, to be combined together in an optimized large-area device after obtaining the results from both experimental thrusts. The design space optimization focused on the pitch of the DMOSFET cell, examining gate length, JFET spacing, and N+ source contact length effects on the device performance. Fig. 2 shows a representative cross section of the DMOSFET, with the various regions of interest being highlighted. A short gate length

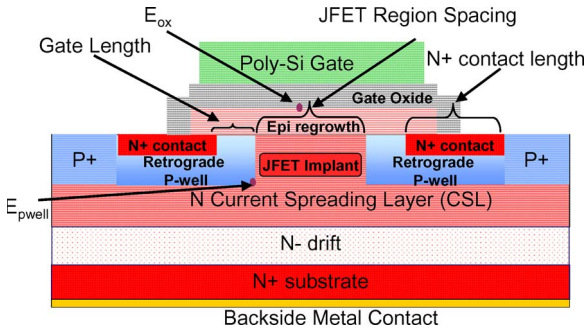

Fig. 2. DMOSFET cross-sectional view, showing the device geometries that were varied experimentally and points where $E_{\rm ox}$ and $E_{\rm pwell}$ were calculated in numerical simulation.

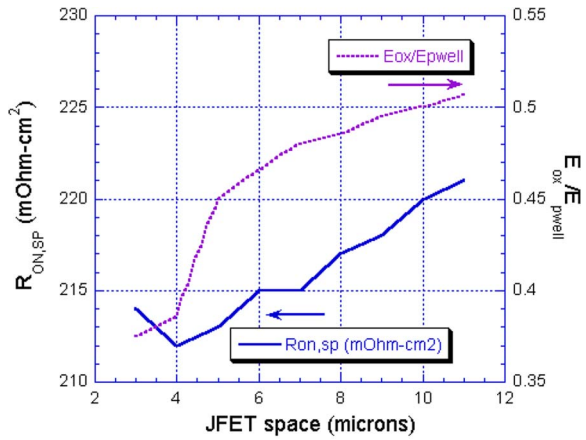

Fig. 3. Analytical model of specific on-resistance and $E_{\rm ox}/E_{\rm pwell}$ plotted against JFET spacing. The model assumes a low-doped 100-μm drift and a 1-μm (1×10^{16}-cm^2) CSL.

can substantially reduce the channel resistance, but this has a limited benefit to the overall on-resistance of 10-kV devices because of their high drift resistance and must be counterbalanced by concerns of possible problems associated with short-channel devices, such as drain-induced barrier lowering causing premature breakdown. This factor motivated an exploration of gate lengths of 1.0 and 1.5 μm in addition to a channel length of 0.5 μm. The JFET spacing is a critical parameter, as too small of a spacing will increase resistance by impeding all current flow, whereas too large of a JFET space not only hurts on-resistance by increasing the device pitch but also increases the electric field seen by the gate oxide above the JFET region, causing reliability issues. Fig. 3 shows a numerical model of this effect, with specific on-resistance and $E_{\rm ox}/E_{\rm pwell}$ (the ratio of the electric field in the gate oxide interface at the center of the cell to the field seen at the bottom corner of the p-well) plotted as a function of JFET spacing. This model shows a minimum in specific on-resistance with a 4-μm JFET space, whereas the corresponding experimental design space included JFET spacings of 4, 5, and 6 μm. It should be noted that, in addition to the low-doped thick drift layer needed for 10-kV devices, the numerical model assumes the use of a 1-μm-thick current spreading layer (CSL) doped at 1×10^{16} cm^{-3}. This CSL layer is essential for allowing the current to spread underneath the p-well region prior to entering the low-doped drift and minimizing the spreading resistance of the device and

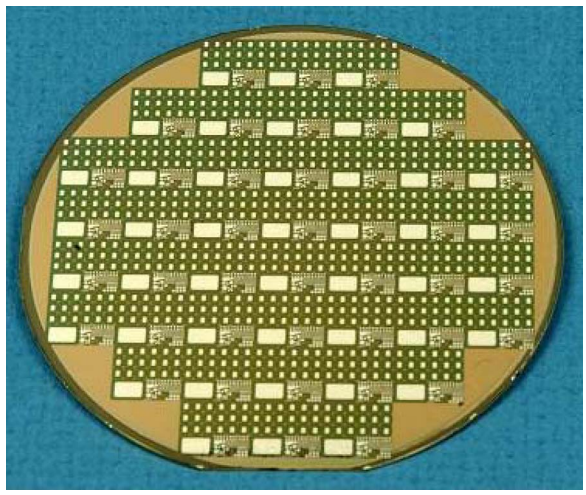

Fig. 4. Image of the completed wafer with 18 DMOSFET geometry variations per reticle.

is also a major factor in determining the JFET resistance of the device. To further explore the impact of the doping level in the CSL/JFET, an additional experimental split was incorporated to implant one wafer with nitrogen (at 195 keV and 2.6×10^{12}-cm^{-2} dose) to create a buried 1×10^{17} cm^{-3} region in the JFET space. The last variable was the source contact length, which is desired to be small to increase device pitch but large enough that source contact resistance is negligible.

Two 4H-SiC wafers were processed with these interleaved design splits, creating 18 different small-area device designs (each with an active area of 0.0029 cm^2) in each reticle, with an additional 19th larger-area device (0.07-cm^2 active area) that used the largest design rules and filled the remaining available space on the reticle. One wafer received the aforementioned JFET implant while the other did not, and all other processes remained identical for both wafers. The starting wafers used a 100-μm epitaxial layer doped at 5×10^{14} cm^{-3}, along with a 1-μm 1×10^{16}-cm^{-3} CSL, and the p-wells were formed with a retrograde implantation of aluminum. The gate oxide was formed using N_2O, creating a 400-Å-thick layer. Because the channel optimization work was being performed in parallel with this experiment, these wafers did not use the epitaxial regrowth process above the implanted p-well. The channel length was defined using standard stepper lithography, comprising the spacing between the edges of the n+ and p-well implants, respectively, down to a length of 0.5 μm without the use of self-aligned techniques. The p+ contact to the p-well was 0.75 μm wide. An n-type doped polysilicon gate was used with a 0.5-μm overlap above the n+ region. The source contacts were formed using nickel silicide, whereas an aluminum layer formed the final metallization. Fig. 4 shows an image of a completed wafer, and Fig. 5 shows the averaged specific on-resistances for all devices on the wafer without the additional JFET implantation. While the primary driver of resistance was the gate length and total device pitch, no adverse affect on breakdown was observed for the shorter channel devices. Likewise, the ON-state resistances decreased with JFET spacing and N+ source contact length. The "Big" device on the reticle had a larger specific on-resistance because its size allowed it to benefit less from the

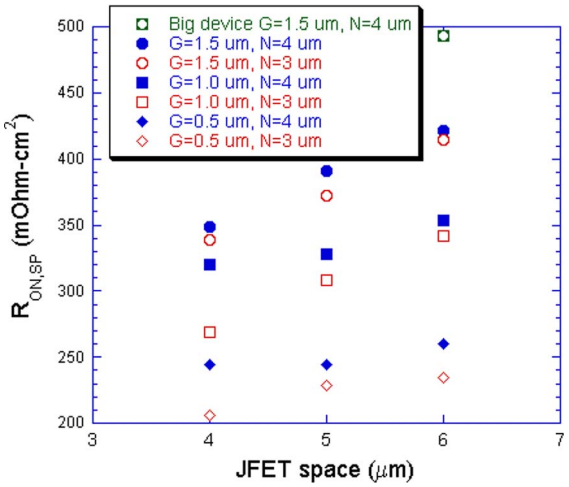

Fig. 5. Specific on-resistances for the 10-kV DMOSFET geometry design space experiment.

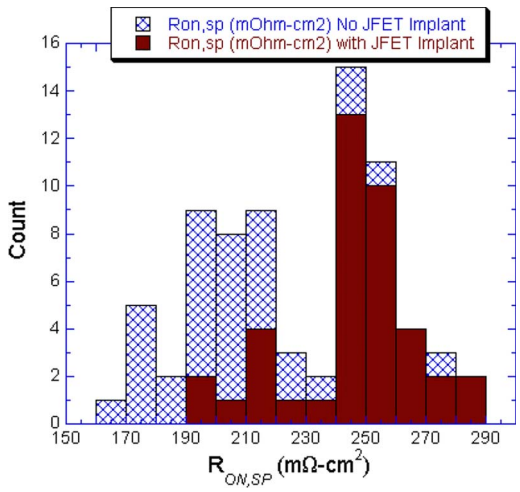

Fig. 6. Histogram of specific on-resistance for the smallest geometry devices (JFET space $= 4$ μm, gate length $= 0.5$ μm, and N+ source length $= 3$ μm) for the wafer with and without a JFET implantation.

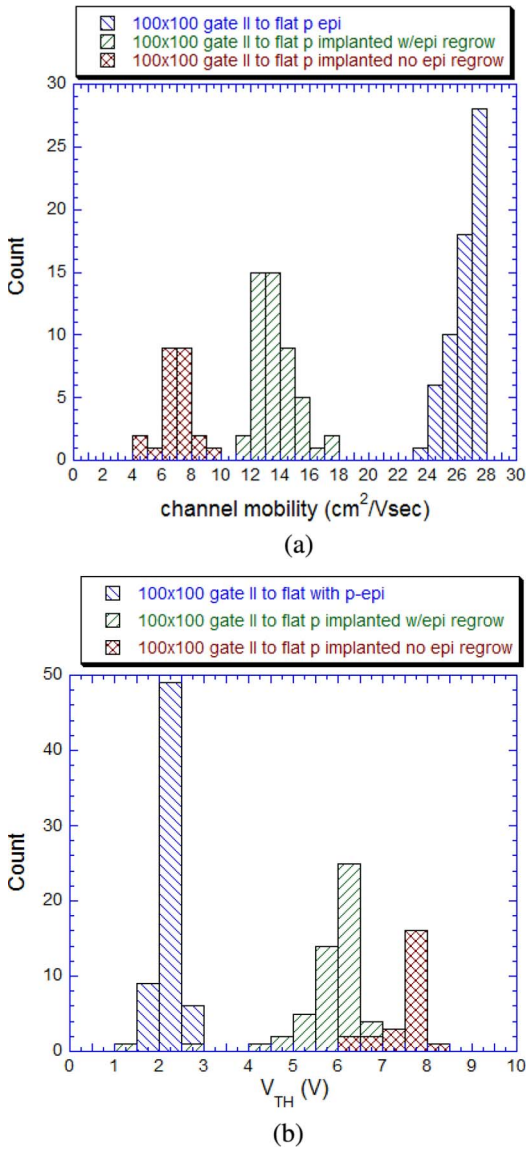

Fig. 7. (a) Histogram of mobilities for $W/L = 100$-μm/100-μm devices grown on a wafer with p-epitaxy, a wafer with an implanted p-well, and a wafer with an epitaxial regrowth on top of an implanted p-well. (b) Histogram of $V_{\rm TH}$ for $W/L = 100$-μm/100-μm devices grown on a wafer with p-epitaxy, a wafer with an implanted p-well, and a wafer with an epitaxial regrowth on top of an implanted p-well.

spreading current through the low-doped drift region compared to the small DMOSFETs. The conclusion reached from these results was that the smaller geometries explored were not detrimental to OFF-state performance but could be used to take advantage of the resulting minimized on-resistance.

Because the wafer without the JFET implant showed negligible JFET resistance, it was expected that the simultaneously processed wafer with the JFET implant would show similar results. However, the wafer with the JFET implant demonstrated remarkably higher resistances across all devices. Fig. 6 shows a histogram of the specific on-resistances for all of the smallest geometry devices on both wafers (JFET space $=$ 4 μm, gate length $= 0.5$ μm, and N+ source length $= 3$ μm). The mean specific on-resistance of these devices on the wafer without the JFET implant was 209 m$\Omega \cdot$ cm^2, but 248 m$\Omega \cdot$ cm^2 was observed for the wafer with the JFET implant. As the on-wafer lateral MOSFET test structures showed very similar mobility results for both wafers and, according to the data received from the vendor, the wafers' drift doping and thickness values were virtually identical, the variation between results is attributed to the act of implantation itself. It is hypothesized that the JFET implantation caused a significant amount of damage that was not removed during the implant anneal process.

In parallel with the DMOSFET geometry optimization, small lateral MOSFETs were also being created to optimize the MOS channel characteristics. It was hypothesized that the damage from the implanted p-well could not be fully removed during the activation annealing. An epitaxial layer grown after the implant, however, could serve to move the channel away from this damage and significantly improve device performance. Additionally, a N_2O gate oxidation process could be employed, which does not have the same rigorous safety requirements that accompany the commercial use of NO and is thus easier to implement.

Fig. 7(a) shows a histogram of mobilities measured on the lateral MOSFETs ($W/L = 100$ μm/100 μm) from three

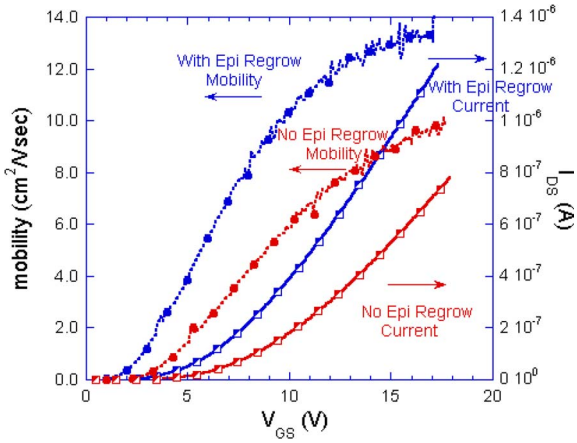

Fig. 8. I_{DS} and transconductance mobility plots as a function of V_{GS} for representative 100-μm/100-μm MOSFETs with implanted p-wells and with or without an epitaxial regrowth process.

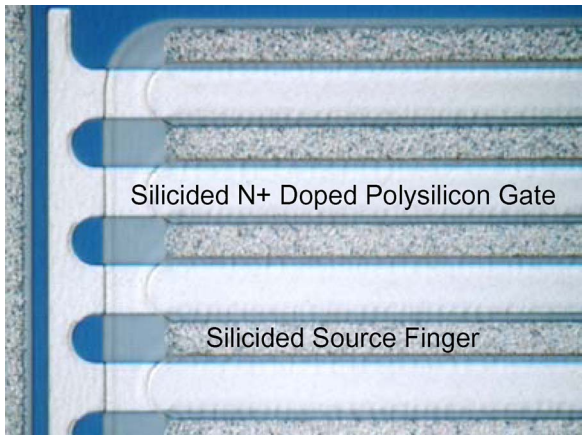

Fig. 9. Image of a portion of the fabricated 0.15-cm^2 active (0.43-cm^2 chip area) DMOSFET with a gate length of 0.5 μm and a pitch of 10 μm.

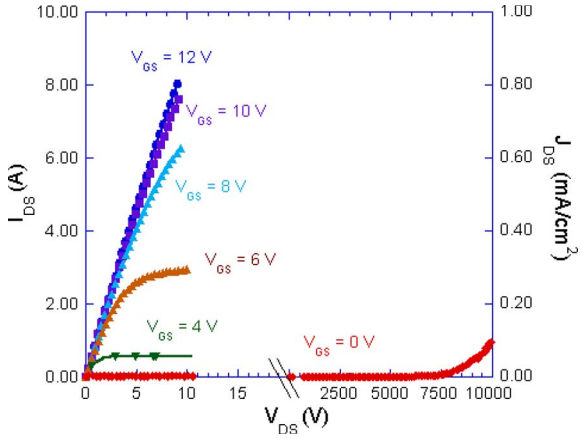

Fig. 10. ON-state and breakdown characteristics of a 0.15-cm^2 active 0.43-cm^2 chip-area DMOSFET.

different SiC wafers. All wafers used similar process sequences, including the N_2O gate oxide formation, with the exception that one wafer formed the devices on a 5-μm p-epitaxial layer, whereas the other two used aluminum-implanted p-wells. Of these two implanted p-well wafers, one, in turn, received an epitaxial regrowth process, growing ~700 Å above the p-well. The histogram shows distinct populations for each of the process conditions, with the implanted p-well alone greatly decreasing the mobility of the devices compared to the undamaged epitaxial p-layer. The addition of the epitaxial regrowth has essentially doubled the measured mobility of devices on an implanted p-well, although still being only about half the mobility of the "ideal" case of the devices on the p-epitaxial material. In a similar fashion, the V_{TH} of the devices has been lowered by the incorporation of the epitaxial regrowth, with the histogram in Fig. 7(b) showing the highest V_{TH} for devices on an implanted p-well and the incorporation of an epitaxial regrowth acting to decrease the V_{TH} by approximately 2 V. The devices on the p-epitaxial material, with the least damage and associated fixed charge, have the population with the lowest V_{TH}.

Fig. 8 shows the I_{DS} versus V_{GS} behavior of two representative devices on implanted p-wells, comparing current and transconductance values between devices with and without the epitaxial regrowth process. When using the epitaxial regrowth, the mobility has nearly doubled, increasing from a peak of 9.8 to 13.2 cm^2/V $\cdot$ s, and the current has increased by a factor of approximately 1.7 times due to both the increase in mobility and the reduction in V_{TH}. This performance, while not generating as high values of channel mobilities as an NO process, is sufficient for the needs of a 10-kV DMOSFET process, and these results were combined with the results from the device geometry experiment to create an optimum design for large-area 10-kV DMOSFETs.

IV. Fabrication and Measurements of Large-Area DMOSFETs

Incorporating the results of the optimization experiments, large-area 10-kV DMOSFETs were fabricated. Of those fabricated, the most promising design used a gate length of 0.5 μm in a cell pitch of 10 μm. The drift remained 5×10^{14} cm^{-3} and 100 μm thick, with a 1-μm 1×10^{16} cm^{-3} CSL, and a mesa etch process was used to etch around the active area of the device through the CSL and to the drift region. A retrograde Al-implanted p-well was used with an epitaxial regrowth layer of ~1000 Å, followed by a N_2O gate oxide process forming a 400-Å-thick layer. A N+ doped polysilicon gate was used with a self-aligned nickel silicidation process, and the source contacts were also formed using nickel silicide. A three-zone JTE was used with an extent of 750 μm, and the resulting chip was 0.42 cm^2, with a 0.15-cm^2 active area. Fig. 9 shows an image of the device fingers prior to final passivation and metallization, showing the linear cell design.

The forward I–V and corresponding reverse breakdown J–V for one of these devices is shown in Fig. 10. With 12 V applied to the gate (3 MV/cm), this device achieved 8 A at 9 V V_{DS} and a current density of 53 A/cm^2 while generating 480-W/cm^2 waste heat, which is well below the reasonable limit of 750 W/cm^2 for current packaging technology that uses liquid cooling [10]. The breakdown voltage of this device is excellent, with only 0.1 mA/cm^2 of leakage at 10 kV and demonstrating the breakdown margin built into the device that

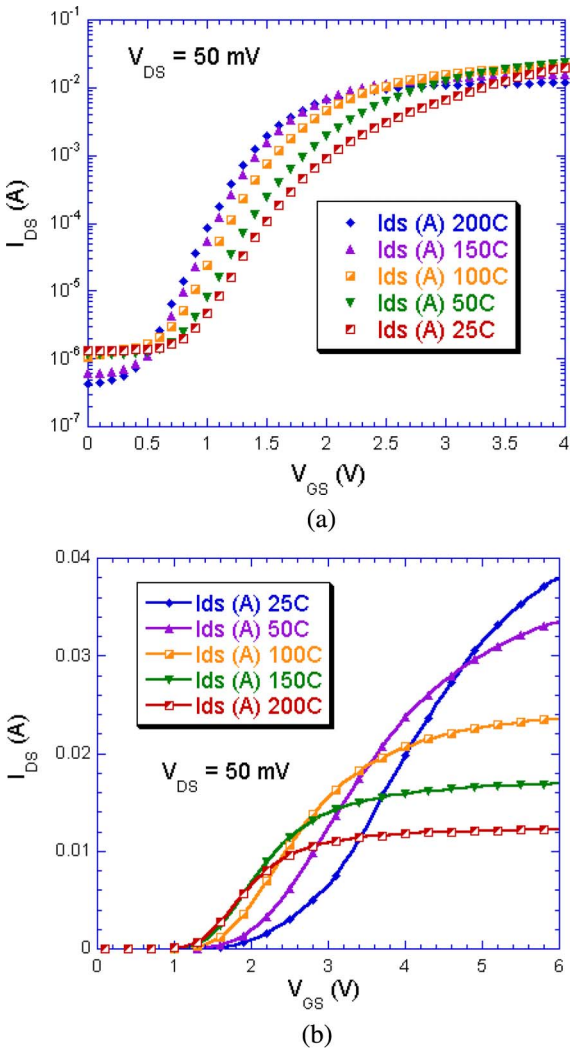

Fig. 11. (a) $I_{\rm DS}$–$V_{\rm GS}$ subthreshold characteristics of a 0.15-cm^2 active 0.43-cm^2 chip-area DMOSFET across a 25–200 °C temperature range. (b) $I_{\rm DS}$–$V_{\rm GS}$ linear characteristics of a 0.15-cm^2 active 0.43-cm^2 chip-area DMOSFET across a 25–200 °C temperature range.

was previously described in Section II. The leakage current does begin to increase after 7500 V, as minor defects within the SiC epitaxial structure allow the beginning of avalanche breakdown.

The measured temperature response of the device is also excellent, with no shifting of its subthreshold current as a function of temperature. Fig. 11 shows the $I_{\rm DS}$ versus $V_{\rm GS}$ of this device for temperatures ranging from 25 °C to 200 °C and for $V_{\rm DS} = 50$ mV. As the temperature increases, the threshold voltage decreases, but that is due to the increasing sharpness of the subthreshold characteristic, and there is no appearance of a charge-induced shift in the subthreshold current. The subthreshold swing S is shown by Sze [11] to be

$$S = \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_D}{C_{\rm ox}}\right) \cdot \frac{1 + \left(\left(C_D + qD_{\rm it}\right)/C_{\rm ox}\right)}{1 + \left(C_D/C_{\rm ox}\right)} \quad (1)$$

where C_D is the depletion capacitance, $C_{\rm ox}$ is the oxide capacitance, and $D_{\rm it}$ is the interface trap density. A steeper subthreshold I–V characteristics equates to a lower S, and MOSFETs

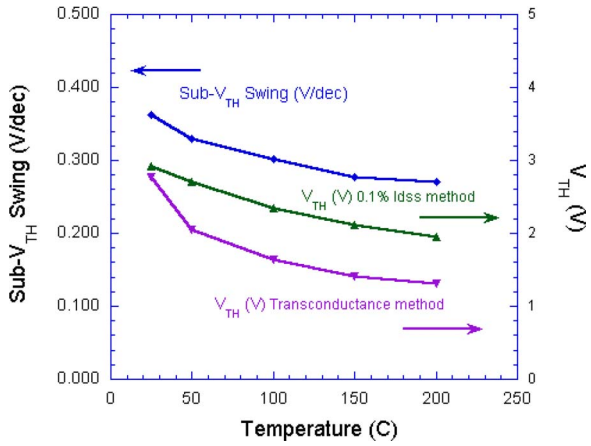

Fig. 12. Measured subthreshold swing and threshold voltage as a function of temperature for the 0.15-cm^2 active 0.43-cm^2 chip-area DMOSFET across a 25–200 °C temperature range.

with high levels of interface traps, as is common for SiC, have increased values for subthreshold swings and shallower subthreshold I–V characteristics. The increasing subthreshold slope and decreasing swing observed in Fig. 11 indicate a significant decrease in $D_{\rm it}$ with temperature, particularly because an increase in temperature by itself acts to increase S.

Aside from the subthreshold swing, the other major characteristic associated with this region is the possibility of a charge-induced shift. This normally occurs due to fixed charge and is observed in lateral shifts in the subthreshold I–V characteristics and corresponding shifts in threshold voltage by the relationship $V_{\rm shift} = -Q_{\rm fixed}/C_{\rm ox}$. In SiC MOSFETs, this fixed shift has been observed to have an additional temperature dependency, with the shift appearing as temperature is increased [5].

The presence of a temperature-controlled charge-induced lateral shift in the subthreshold characteristics would cause the device to begin to turn on as temperature increased, despite the gate remaining at 0 V. In contrast, the device shown in Fig. 11 has a leakage current (at $V_{\rm DS} = 50$ mV) that decreases with increasing temperature, from 1 μA (6.7 μA/cm^2) at $V_{\rm GS} = 0$ V and 25 °C to 0.4 μA (2.7 μA/cm^2) at $V_{\rm GS} = 0$ V and 200 °C. Because this device does not experience a charge-induced lateral shift on the $I_{\rm DS}$–$V_{\rm GS}$ curve as a function of temperature, there is no additional contribution to the avalanche breakdown current at higher temperatures from an undesirable temperature-controlled partial turn-on of the device that could otherwise significantly lower the resulting breakdown voltage. Fig. 12 shows the subthreshold swing and threshold voltage of the device as a function of temperature, with the threshold voltage being plotted as determined by the transconductance method and as defined by the point where the drain current is equal to 0.1% of the maximum current. The threshold voltage tracks the subthreshold swing values, as it decreases due to the steepening of the slope, which is caused by the filling of traps at higher temperature with the higher numbers of intrinsic carriers.

The specific on-resistance of the device has also been evaluated, as shown in Fig. 13, with the experimental data being compared to an analytical model of the DMOSFET presented

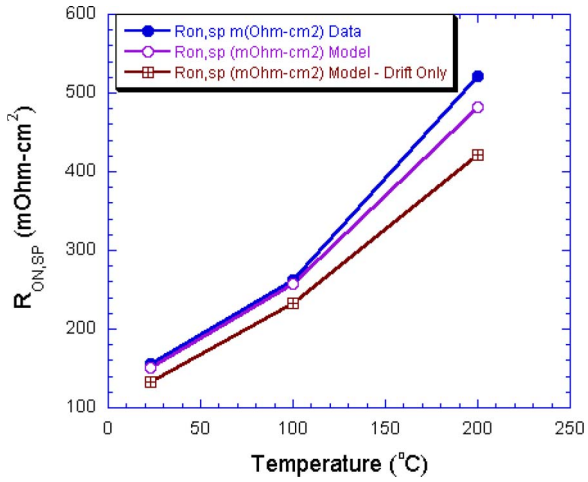

Fig. 13. Measured specific on-resistance for the 0.15-cm^2 active 0.43-cm^2 chip-area DMOSFET across a 25–200-°C temperature range as a function of temperature compared to the analytical model.

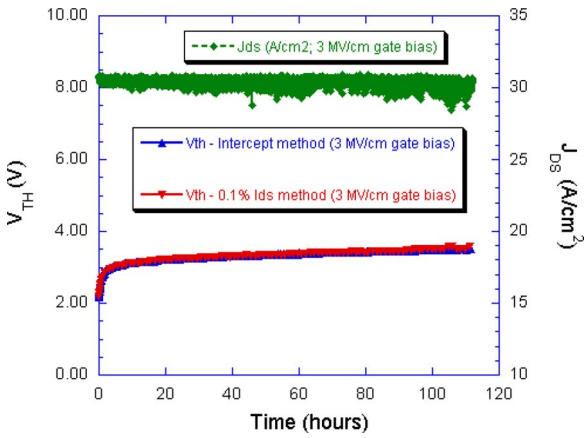

Fig. 14. Stressing of DMOSFET with epitaxial regrowth layer on p-well implant. Stressed at $V_{\rm GS} = 12$ V (3 MV/cm) and $V_{\rm DS} = 12.5$ V.

by Baliga [12]. The primary component of the device resistance remains the drift resistance, with the MOS channel and the rest of the device components forming 15%–20% of the total device resistance. The initial impact of heating is minimized as traps are filled to counteract the normal decrease in mobility for majority carrier devices, which is why the proportion of resistance in the MOS channel does not substantially increase until the 200-°C data point. A corresponding lateral MOSFET was measured with mobilities of 13, 10, and 3.2 cm^2/V · s at 27 °C, 100 °C, and 200 °C, respectively, demonstrating this impact.

These DMOSFETs have also shown excellent preliminary operational stability as a function of temperature. Fig. 14 shows the results of temperature–bias stress testing on a small-area (0.0029 cm^2 active) test DMOSFET with identical design rules and made simultaneously with the large-area DMOSFET. The device was stressed at $V_{\rm GS} = 12$ V (3 MV/cm) and $V_{\rm DS} = 12.5$ V on a heated chuck held at 200 °C for a period of over 110 h. The threshold characteristics were measured intermittently throughout the test period, and the output current was monitored continually. After an initial increase in $V_{\rm TH}$ of 0.8 V after 5 h, $V_{\rm TH}$ increased by only 0.5 V over the next hundred hours of testing, whereas the output current dropped by 1%.

V. Conclusion

The design and optimization of a large-area 10-kV DMOSFET are presented, with a 0.15-cm^2 active-area (0.43-cm^2 die) device providing 8 A at $V_{\rm DS} = 9$ V (53 A/cm^2 and 480 W/cm^2) and 3 MV/cm on the gate oxide. With the incorporation of an epitaxial regrowth layer above the implanted p-well, excellent subthreshold and stressed performance characteristics were demonstrated across the 25–200-°C temperature range. No subthreshold characteristic shift was observed as a function of increased temperature, resulting in a low OFF-state leakage of 0.4 μA (2.7 μA/cm^2) at $V_{\rm GS} = 0$ V and 200 °C.

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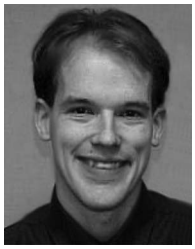

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She was a Postdoctoral Researcher with the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, from 1996 to 1999, developing a pump-probe spectroscopic measurement system using an NSOM, and using this system to measure local carrier dynamics in various semiconductor structures. After her postdoctoral work, she was with Lucent Technology in 1999 (later spun off as Agere Systems), concentrating on the design and measurement of electroabsorption-modulated lasers for fiber-optic telecommunications, as well as on the fiber-optic communication system characterizations of distributed feedback lasers, electroabsorption-modulated lasers, and avalanche photodiodes. Since 2005, she has been with the Compound Semiconductor Research Group, Advanced Materials and Semiconductor Device Technology Center, Northrop Grumman Corporation, Linthicum, MD. While at Northrop Grumman Corporation, she helped design, fabricate, and characterize high-power SiC devices. She has coauthored over 20 publications in various refereed journals and conference proceedings.

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He is currently a Program Director with Northrop Grumman Corporation, Linthicum, MD, where he is responsible for the direction and development of new technology for advanced systems. He is an accomplished and respected Leader in the fields of new materials growth, new device development, and transfer of technology to production. He performed the original work on vapor-phase epitaxy of pure and doped GaAs and InP films for microwave devices, both for millimeter-wave Gunn diodes and X-band MESFETs. Original investigative material work was also performed on the activation of ion-implanted impurities in gallium arsenide and on the impact of subsurface damage on devices fabricated in undoped GaAs substrates. More recently, CVD growth of 6H- and 4H-SiC was pioneered for the pure and doped structures required in the fabrication of the first 4H-SiC MESFET and SIT microwave devices. Recent research areas include GaN–AlGaN CVD, SiC hot-wall CVD, and aluminum nitride bulk crystal growth for microwave applications. Expert in the design of high-voltage microwave transistors, he has authored papers on high-efficiency castellated FETs and high-voltage GaAs power MESFETs. His UHF SiC SITs currently hold the record for the highest reported microwave power and efficiency of any semiconductor material, providing a sixfold improvement in power output per package when compared with commercial GaAs and silicon products.

Ranbir Singh (M'03) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, New Delhi, India, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh.

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Dr. Singh served on the Technical Committee of the International Symposium on Power Semiconductor Devices and ICs from 2002–2004 and was part of a panel to develop a roadmap for the insertion of SiC-based power devices into commercial applications. In 2003, and then again in 2004, he received the IEEJ Technical Development Award for the development of ultrahigh-voltage SiC devices.