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HIGH POWER SIC PIN RECTIFIERS

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High voltage PiN rectifiers made using conventional semiconductor materials such as Silicon are restricted to less than 20 kHz and less 120°C operation, thereby severely limiting the availability of advanced electronic hardware used for power grid (also called electric utility), energy storage, pulsed power, intelligent machinery and ultra high voltage solid state power conditioning. Such applications require high power density, very high frequency, and high temperature rectifiers to realize reasonably sized systems. SiC PiN Rectifiers are expected to play an enabling role in a variety of such high voltage applications because they have been shown to offer 2 to 3 orders of magnitude faster switching, high junction temperature capability, high current density operation, and much higher power densities as compared to Silicon.

1. Introduction

Properties of SiC that enable dramatically improved capabilities for SiC PiN rectifiers include: (a) an order of magnitude higher breakdown electric field; (b) a ~3X wider bandgap; and (c) a ~3X higher thermal conductivity than Silicon. A high breakdown electric field allows the design of SiC power devices with thinner and higher doped blocking layers. The large bandgap of SiC results in a much higher operating temperature and higher radiation hardness. The high thermal conductivity for SiC (4.9°C/W) allows dissipated heat to be readily extracted from the device. Hence, a larger power can be applied to the device for a given junction temperature. However, SiC bipolar rectifiers suffer from a ~3X higher built-in junction voltage drop as compared to Si devices due to SiC's larger bandgap. However, since the on-state voltage drop decreases with increasing temperature, the junction voltage drop difference is reduced to less than 2X as compared to a Si PiN rectifier operating at room temperature for a SiC PiN rectifier operating at 500°C. An important property of SiC from a bipolar device perspective is its indirect bandgap (as opposed to GaN, which has a direct bandgap) which has the potential for high recombination lifetime, if the material is of excellent quality. The wide bandgap of SiC also allows negligible junction leakage currents up to 500 °C in PiN rectifiers. This allows high temperature operation without excessive leakage current or thermal runaway. Cooling requirements, and hence the size and weight, of power electronic systems could be reduced if the systems were designed to take advantage of the ability of SiC rectifiers to operate at elevated temperatures.

To increase the efficiency and decrease the cost, weight and volume of power conversion systems, it is important to reduce the heat generated during device operation. Most of the heating in a rectifier occurs either in the turn-on state or during switching

transients. As in Si, SiC power rectifiers may be broadly classified into majority carrier rectifiers (Schottky rectifiers), in which on-state conduction is dependent on doping and bulk carrier mobilities; and minority carrier rectifiers (PiN rectifiers) which rely on conductivity modulation for on-state current transport. Schottky rectifiers offer extremely fast switching, and although their voltage drop at low current densities can be low, its magnitude increases dramatically at high current densities. This issue increases exponentially in its severity as these rectifiers are designed for higher voltage ratings. This is because the on-resistance of a voltage blocking layer increases exponentially with the designed breakdown voltage. On the other hand, bipolar PiN rectifiers offer low forward voltage drop at high current densities, but have higher switching losses as compared to Schottky rectifiers. Application engineers often ask which SiC rectifier may be suitable in the high voltage range – Schottky rectifier or PiN rectifier. If on-state voltage drop is the only consideration, the current density specification at which this choice can be made is for SiC Schottky and PiN rectifiers for ideal blocking voltage in the 2 to 30 kV range is shown in Figure 1 using generalized assumptions. Above this limit, PiN rectifiers may be more attractive than Schottky rectifiers because it offers lower on-state voltage (V_F) drop. Switching speed of rectifier also plays an important role in determining its appropriateness to a particular application. There often exists a design trade-off between the switching speed and the on-state voltage drop in a bipolar rectifier if lifetime is changed. There exists an upper limit to the current density for rectifiers, which is determined by commercial packaging technology. Conventional power device packaging technology can only dissipate 250-400 W/cm^2 continuously. Since the built-in voltage of 4H-SiC bipolar device is ~3 V, the maximum continuous current may be limited to only 100-150 A/cm^2 [1].

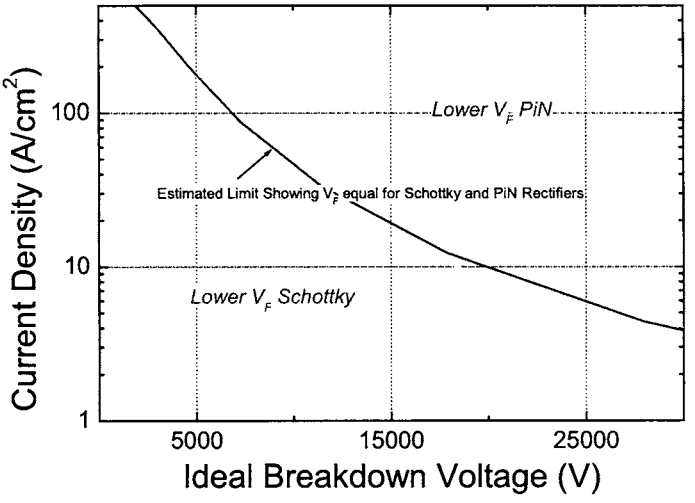

Figure 1: Approximate current density limit where SiC Schottky rectifiers and PiN rectifiers offer similar on-state voltage drop (V_F).

2. PiN Rectifier Design and Operation

SiC PiN rectifiers are fabricated using n^+ wafers with low doped, thick n^- epitaxial layers, which are typically grown over a n^+ epitaxial buffer layer. The p^+ Anode region may be formed by using a highly doped epitaxial layer or by using ion implantation of p-type dopants such as Aluminum or Boron. Typically, PiN rectifiers with epitaxial p^+ Anode as shown in Figure 2 may offer lower on-state voltage drop as compared to ion implanted PiN rectifiers because of high p-type dopant activation, which determines the injection efficiency of current carriers into a low doped, thick epitaxial layer. The blocking voltage of such a rectifier is determined by (a) the doping and thickness of voltage blocking epitaxial layer (i-region) and (b) the effectiveness of the edge termination technique used to fabricate the device. Generally speaking, the current carrying capability depends on the physical area of the device and the minority carrier lifetime in the i-layers. For the device to sustain a high electric field during the reverse bias operation, it is essential to reduce the substrate induced defects, such as micropipes and epitaxially induced defects.

2.1. *High voltage epitaxial layer design*

In order to realize high voltage rating on PiN rectifiers, the doping and thickness design of n^- epitaxial layer is crucial. During reverse bias application, the highest electric field occurs at the p^+/n^- junction, and the gradient of the electric field in the n^- layer is determined by its doping, and the depth to which the electric field extends is determined by its thickness. The doping and thickness of n- epitaxial layer determines the blocking voltage of the device. For a designed voltage blocking capability, an n^- epitaxial design is called a punchthrough design if a finite electric field exists at the n^- layer/n^+ buffer layer junction. On the other hand a non-punchthrough design corresponds to the case where i-layer thickness is equal to or larger than the parallel plane avalanche breakdown width [2]. In a typical ultra high voltage design, a punchthrough design is used in order to keep the thickness of the epitaxial layer reasonable. For such a case, the i-layer thickness

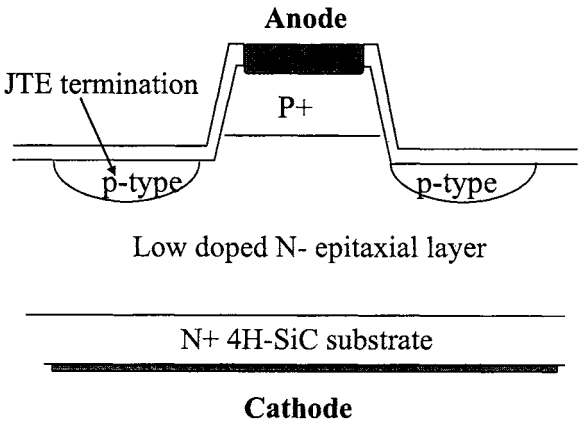

Figure 2: Cross-section of a high voltage 4H-SiC PiN rectifier using a highly doped epitaxially grown Anode layer and etched and implanted JTE structure.

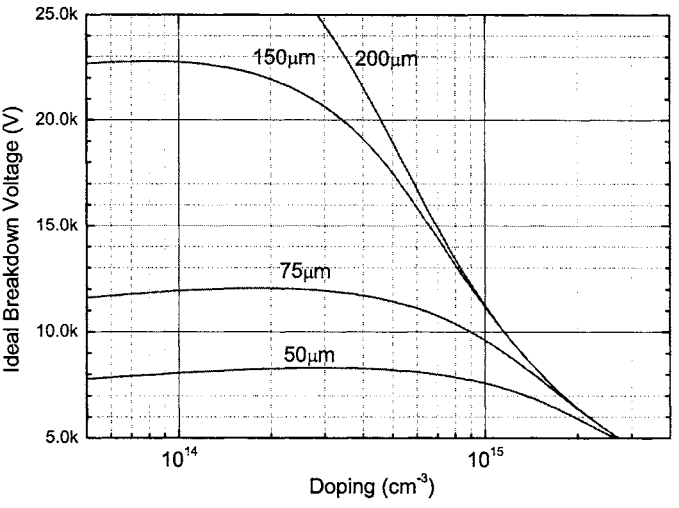

Figure 3 : Ideal blocking voltage as a function of i-layer doping and thickness.

can be derived from basic depletion equation as:

$$W = \frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D} - \sqrt{[\frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D}]^2 - [\frac{2\varepsilon \cdot V_B}{q \cdot N_D}]} \tag{1}$$

where V_B is the device blocking voltage, W is the epitaxial layer thickness, N_D is the doping of the epitaxial layer, q is the elementary charge, ε is the dielectric constant of SiC, and $E_C(N_D)$ is the critical electric field as a function of the i-layer doping. One of the commonly accepted empirically derived relationships showing the dependence of critical electric field with i-layer doping in 4H-SiC is given by [3]:

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log(\frac{N_D}{10^{16}})} \tag{2}$$

Using these formulae, the ideal blocking voltage is plotted as a function of i-layer doping and thickness in Figure 3. The decrease in blocking voltage with a decrease in doping is an artifact of the approximations used in the derivation of E_C, and is not accurate. Since the edge termination design as well as material defects influences the blocking voltage of ultra high voltage devices, very large blocking voltage margins are usually adopted in the design of ultra high voltage PiN rectifiers.

2.2. *Edge termination design*

From a device design standpoint, the biggest technological challenge in achieving high voltage PiN rectifiers is the design and implementation of an effective edge termination. Such a technique is expected to make the electric field distribution uniform

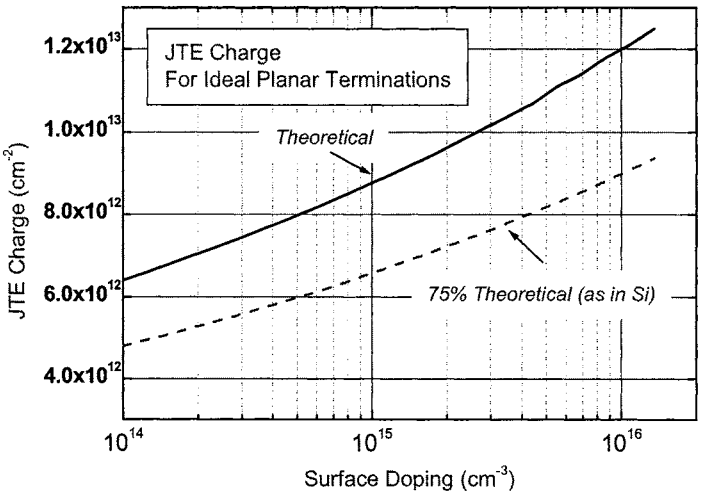

Figure 4: JTE charge vs. surface doping of the voltage blocking layer for a SiC device.

at the edge of the device, approaching the ideal breakdown voltage capability of the epitaxial layer used. Traditionally, many techniques like guard rings, floating field rings, and trench guard rings [4] have been used. Another promising edge termination design involves implanting the device edge with an optimum p-type charge in order to reduce the electric field gradually from the device edge to the outer periphery of the device structure. This technique is called junction termination extension (JTE) [2]. Using the approximations used to derive the critical electric field, the optimum JTE charge is expected to depend on the background doping concentration of the low doped n-type region. A plot showing the ideal total charge per unit area of the implanted JTE region is shown in Figure 4. The design of high voltage Silicon devices made using JTE typically utilize a JTE charge 25% below the ideal predicted charge by theoretical analysis. This is because JTE charge in excess of the ideal value results in a sharp reduction in the obtained breakdown voltage, while a charge smaller than the optimum does not drastically affect the breakdown voltage of the device. The JTE charge corresponding to 75 % is also plotted in this graph for SiC.

2.3. *Effect of lifetime on rectifier on-state voltage drop*

Achieving a high level of carrier lifetimes in the thick, SiC epitaxial layers is critical to obtaining acceptable on-state voltage drop in 4H-SiC PiN rectifiers. For a given blocking voltage design, which determines the thickness of i-layer, epitaxial growth experts need to deliver the required carrier lifetimes in these layers to obtain low on-state voltage drops in these rectifiers. Key lifetime limiting factors in thick epitaxial layers are: (a) compensating dopant species; (b) Unintentional metallic impurities; (c) morphology of the epitaxial layers during and after the growth; and (d) thickness and doping uniformity of thick epitaxial layers. For the extremely thick epitaxial layers used in these rectifiers, hot wall epitaxial reactors were used. Using these reactors, higher carrier lifetimes can be obtained.

The dominant components in the on-state voltage drop in a PiN rectifier are given by:

$$V_F = V_{P+Cont.} + V_M + V_{P+N-} + V_{N+N-} + V_{Subs} \quad (2a)$$

where V_F is the on-state voltage drop in a PiN rectifier, $V_{P+Cont.}$ is the p+ contact resistance V_M is the 'middle region' (i-region) voltage drop, V_{P+N} and V_{N+N-} are the junction drops at p^+ n^- and n^+ n^- junctions, and V_{Subs} is the resistive voltage drop in the substrate. The voltage drop in the i-layer (V_M) is determined by the extent of carrier modulation in the i-region of the PiN rectifier. Using a broad approximation, the i-region voltage drop is related to the carrier lifetime by the following relationship [2]:

$$V_M = \frac{3kT}{q}\left(\frac{W}{2L_a}\right)^2 \quad \text{for } W \leq 2L_a \quad (3)$$

$$V_M = \frac{3\pi kT}{8q} e^{\frac{W}{2La}} \quad \text{for W} \geq 2L_a$$

where k and T are Boltzmann's constant and operating temperature. L_a is the ambipolar diffusion length, which is given by $L_a = \sqrt{D_a \tau_{HL}}$. D_a is the ambipolar diffusion constant given by $D_a = \mu_a \cdot \frac{kT}{q}$, and τ_{HL} is the high level carrier lifetime. The ambipolar carrier mobility, μ_a is given by $\mu_a = \frac{\mu_n \mu_p}{\mu_n + \mu_p}$. Here, μ_n and μ_p are the minority carrier electron and hole mobility in the voltage blocking layer.

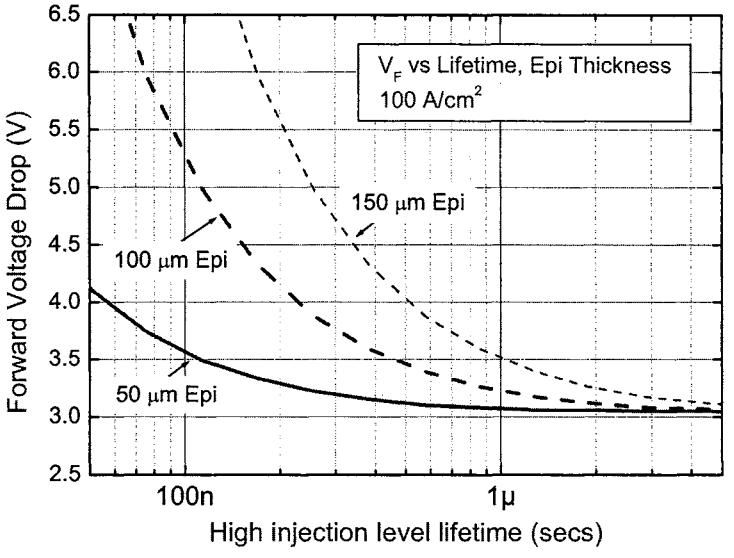

Figure 5: Forward voltage drop in PiN rectifiers as a function of lifetime and epitaxial thickness.

V_{P+N-} and V_{N+N-} are dependent on the minority carrier concentrations at the two end-regions of the n^- layer. A detailed analysis of these voltage drops requires an iterative solution [2], which is not very easily calculated. If a reasonably high injection level is assumed, the sum of these end-region voltage drops can be estimated to be equal to the turn-on voltage of the SiC p^+ n^+ junction. Resistive drops like V_{Subs} and $V_{P+Cont.}$ are not trivial in bipolar device like PiN rectifiers because of extremely high current densities that typically flow through these devices, as compared to majority carrier devices like Schottky rectifiers. The on-state voltage drop of a PiN as a function of carrier lifetime and epitaxial layer thickness is plotted in Figure 5. This figure shows that a higher carrier lifetime results in better conductivity modulation, with on-state voltage drop approaching the built-in voltage drop of a p^+ n^+ junction. A thicker epitaxial layer requires a higher carrier lifetime in order to achieve a lower on-state voltage drop PiN rectifier. However, it is encouraging to note that beyond a carrier lifetime of 3 μs, even a 150 μm epitaxial layer is well modulated, because the i-region voltage drop is negligible as compared to the total voltage drop of the diode. Since this carrier lifetime is more than two orders of magnitude smaller than Si devices with comparable blocking voltage ratings, SiC is expected to offer extremely high switching speeds.

2.4. *Carrier lifetime measurements in SiC PiN rectifiers*

Carrier lifetimes in the thick n^- voltage blocking layers of PiN rectifiers are frequently measured using the switching characteristics of these rectifiers. When the rectifier is switched from its current carrying on-state to its voltage-blocking off-state with the application of reverse bias, the current flowing through the rectifier gradually decreases, and then reverses before reducing to zero. This is referred to as the reverse recovery waveform of the rectifier. The magnitude and the rate of decay of the reverse current is determined by the thickness, doping and minority carrier lifetime of the n- voltage blocking layer as well as the on-state current flowing through the rectifier before it was switched. The technique to extract a value for carrier lifetime in the n- voltage blocking layer from the exponential decay tail of the current waveform is called the current recovery technique (CRT) or the Lax-Neustadter's technique [5].

However, the CRT fails frequently when applied to SiC rectifiers because it assumes a uniform carrier lifetime in the entire n-voltage blocking layer of a PiN rectifier [6]. It is often observed that the carrier lifetime in a thin layer close to the PN junction is significantly lower than that in the bulk of the n-voltage blocking layer. This observation may be explained with the assumption that the high-temperature growth of a heavily doped p^+-emitter leads to a dramatic reduction in the carrier lifetime in a thin layer near the p^+n^- junction, where the local lifetime τ^* is much shorter than bulk carrier lifetime, τ_p. In [7], the minority carrier lifetime τ_p was measured by Open Circuit Voltage Decay (OCVD) technique. It is well known that CRT gives the local lifetime near the p^+n_o junction. Hence, τ^*, instead of τ_p, is measured by CRT in this case. Figure 6 shows a pulsed isothermal I-V characteristic of a 4H-SiC rectifier with an Anode area of 0.08 cm^2, voltage blocking n-layer thickness of 150 μm and a blocking capability of 10 kV at room temperature. At j_f = 180 A/cm^2, the rectifier differential resistance $r_d = dV/dj_f$ = 1.6×10^{-2} Ohm cm^2. Meanwhile, the ohmic resistance of unmodulated base must be $r_n = W/q\mu_n n_o$ = 0.39 Ohm cm^2, i.e., 24 times

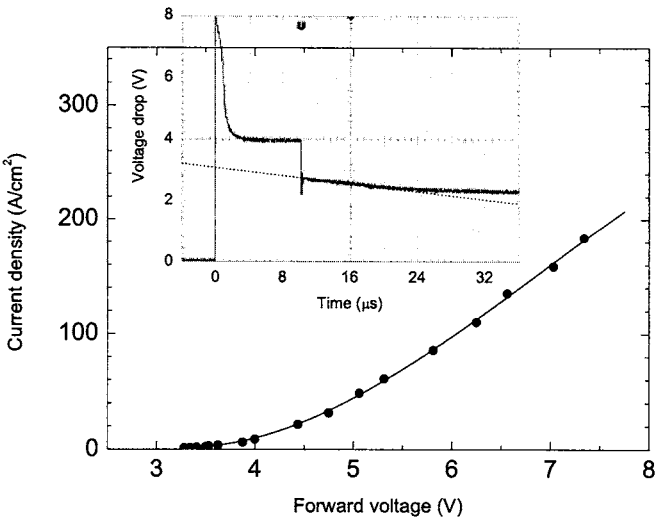

Figure 6: Forward current–voltage characteristic of a 10 kV 4H-SiC rectifier. Inset shows the time diagram of voltage drop across the rectifier during the OCVD measurements. Forward current I_f = 0.6 A (j_f = 7.5 A/cm^2).

the experimentally observed value at μ_n = 800 cm^2/Vs and net donor concentration, n_o = N_d - N_a = 3×10^{14} cm^{-3}. Hence, the I-V characteristic demonstrates directly the high level of base modulation. Inset in Figure 6 shows voltage-time diagram of OCVD process. At t = 0, the pulse of forward current, with amplitude I_f = 0.6 A (j_f = 7.5 A/cm^2), is applied to the rectifier connected in series with a 50-Ohm load. It is easy to verify that this j_f value ensures a high injection level in the base. As seen in the inset, the steady state is attained in about 4 μs, which indicates that the τ_p value is 1.4-1.8 μs. After the termination of the current at t = 10 μs, all "classical" phases of the post-injection voltage decay are observed [8]: (i) abrupt change in voltage just after current termination, (ii) voltage decay linear in time, and (iii) exponential voltage decay at the final stage. At high injection level, simplified analysis of the OCVD curve [9] gives for τ_p the following expression:

$$\tau_p = -\frac{2kT}{q}\left(\frac{dV}{dt}\right)^{-1} \tag{4}$$

where dV/dt is the slope of the linear part in the voltage decay curve. In this case, τ_p = 1.55 μs at T = 293 K.

The ambipolar diffusion length L_a is defined by $L_a = \sqrt{D\tau_p}$, where D = $D_p 2b/(b+1)$. Here D_p is the hole diffusion coefficient, $b = \mu_n/\mu_p$ (μ_n and μ_p are the electron and hole mobilities, respectively). With μ_n = 800 cm^2/Vs, μ_p = 100 cm^2/Vs, and D_p = 2.5 cm^2/s, L_a is calculated to be about 26 μm at T = 300 K.

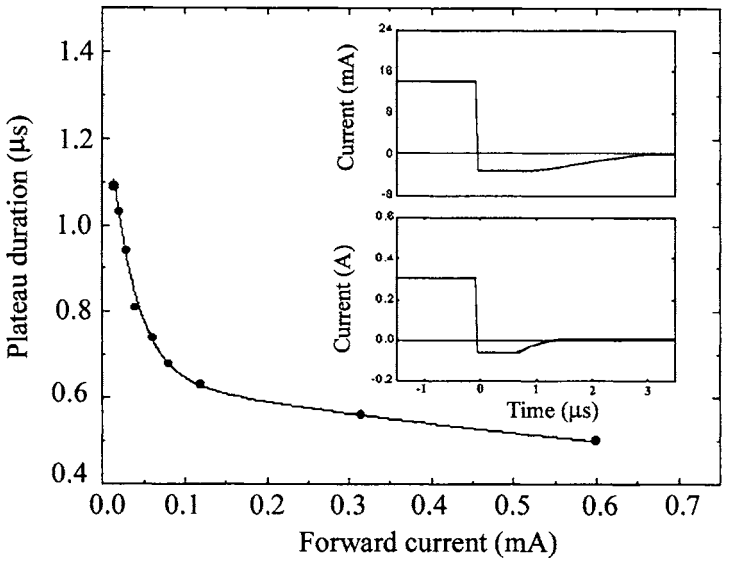

Figure 7: Dependence of the plateau duration in CRT measurements on the forward current I_f at $I_f/I_r = 5$. Inset shows the time dependences of current waveform at two forward current amplitudes: (a) $I_f = 12$ mA, (b) $I_f = 0.6$ A. $I_f/I_r = 5$ for both curves.

The inset in Figure 7 shows current-time diagrams during CRT measurements at $I_f =$ 12 mA and $I_f = 300$ mA. Pronounced reverse current "plateaus" with duration of 0.4 μs for $I_f = 300$ mA and 1.1 μs for $I_f = 12$ mA were observed. For both curves in the inset of Figure 7, the ratio $I_f/I_r = 5$. According to the "classical" theory of CRT [5], the plateau duration must be equal to the lifetime τ_p at this I_f/I_r ratio if the injection level is low. At high injection levels, the plateau duration must decrease monotonically with increasing I_f even at the same I_f/I_r ratio [10]. Figure 7 shows the dependence of the plateau duration on the forward current I_f at $I_f/I_r = 5$. As seen, the plateau duration decreases monotonically with increasing I_f, in agreement with the prediction of the theory. It is noteworthy that at the minimum current of 12 mA, the plateau duration (1.1 μs) is only slightly shorter than the τ_p value measured by OCVD.

It is well known that the following conditions should be satisfied for the classical CRT technique to be applicable: (i) the injection level is to be low, and (ii) the injection coefficient of the emitter should be equal, or very close to unity. To provide a low injection level, the condition $p(0) << n_o$ should be satisfied. For the injection coefficient to become close to unity, the recombination current in the Space Charge Region (SCR) of the $p^+ n^-$ junction is to be low enough, with the ratio $I_{rec}/I_{diff} << 1$. Assuming $p(0) = n_o$, we can obtain for rectifiers with $W/L >> 1$ the following expressions for j_{diff} and j_{rec} [11]:

$$j^*_{diff} = qN\frac{\sqrt{D_p}}{\sqrt{\tau_p}}, \qquad j^*_{rec} = \frac{N}{n_i} j_{ro}. \tag{5}$$

where n_i is the intrinsic carrier concentration, and j_{ro} is the pre-exponential factor of the SCR recombination current.

With $N = 3\times10^{14}$ cm^{-3}, $D_p = 2.5$ cm^2/s, and $\tau_p = 1.55$ μs, the condition (i) is satisfied at $j_{diff} << 6\times10^{-2}$ A/cm^2 ($I_{diff} << 5$ mA). It is noteworthy that the minimum current of 12 mA apparently corresponds to an intermediate injection level. The maximum current of 300 mA corresponds to a very high injection level. Assuming that:

$$\frac{j^{\bullet}_{rec}}{j^{\bullet}_{diff}} = \frac{j_{ro}}{qn_i}\sqrt{\frac{\tau_p}{D_p}} << 1 \tag{6}$$

Calculations based on these formulae show that j_{ro} (with $n_i = 10^{-8}$ cm^{-3}, $D_p = 2.5$ cm^2/s, and $\tau_p = 1.55$μs), must be much less than 2×10^{-24} A/cm^2. The reported j_{ro} values for 4H-SiC rectifier rectifiers fall within the range between 10^{-25} A/cm^2 and 10^{-22} A/cm^2 [12, 13]. So the condition (ii) can only be satisfied in rectifiers with j_{ro} close to the minimum observed values.

2.5. *PiN rectifier operation under superhigh current densities*

An important application area for SiC PiN rectifiers is under very high current density conditions in pulsed modes such as radars, directed energy weapons, space based lasers, space exploration, and electromechanical guns. In such applications, extremely high current density operation is required. At high current densities the forward voltage drop across the rectifier is determined by nonlinear processes, such as electron-hole scattering [14, 15] and Auger recombination [16], and the dependence of emitter efficiency on current density [17]. The contribution of various nonlinear processes to the current-voltage characteristic has been investigated in detail for Silicon thyristors and rectifiers (see, for example, Ref. [18]). However, for Silicon carbide devices, these processes were explained for the first time in Ref [19]. The non-ideality of the emitter p^+-n junction is considered to explain experimental results at superhigh current densities. In the framework of the theory [17], the properties of junctions are described by introducing saturation current densities, j_{ns} and j_{ps}:

$$j_{ns} = q\sqrt{\frac{D_n}{\tau_n}}\cdot\frac{n_i^2}{N_a} \tag{7}$$

where D_n, τ_n, N_a are the diffusion coefficient of electrons, electron lifetime, and acceptor concentration in the p^+-emitter, respectively; and n_i is the intrinsic concentration. The saturation leakage electron current density of the N-n^+ junction, j_{ps}, is defined similarly. The value $j_{ps} = j_{ns} = j_s$ is an essential fitting parameter of the theory, characterizing the quality of the emitter junctions.

In Silicon rectifiers, j_s lies commonly in the range 10^{-14}-10^{-12} A/cm^2 [17]; in GaAs rectifiers, j_s is within the range 10^{-18}-10^{-16} A/cm^2 [20] owing to the fact that the band gap in GaAs ($E_g = 1.4$ eV) is larger than that in Si ($E_g = 1.1$ eV). It can be calculated from the very wide SiC band gap, the leakage current j_s is as small as ~10^{-45}A/cm^2 at 300 K. In the framework of the theory [17], the total voltage drop $V(j)$ at a given current density j is calculated as a sum of voltage drops across the contacts to a structure, V_c, the emitter junctions, V_e, and the rectifier base, V_b:

$$V = V_c + V_e + V_b. \tag{8}$$

The voltage drop across the contacts of the structure, V_c, is given by:

$$V_c = 2R_c j \tag{9}$$

where R_c is the contact resistivity. The voltage drop across the emitter junctions, V_e is given by:

$$V_e = \frac{kT}{q}\ln\frac{p_o p_W}{n_i^2} = \frac{2kT}{q}\ln\frac{j}{j_o} \tag{10}$$

where:

$$j_o = \frac{qDn_i}{2L}\cdot\frac{b+1}{\sqrt{b}}\left[\left(1+\sqrt{1+4jj_{ns}\frac{b}{b+1}\left(\frac{L}{qDn_i}\right)^2}\right)\cdot\left(1+\sqrt{1+4jj_{ns}\frac{1}{b+1}\left(\frac{L}{qDn_i}\right)^2}\right)\right]^{1/2}. \tag{11}$$

Here p_o (j) and p_W (j) are the boundary hole concentrations in the n-base at p^+-n and N-n^+ junctions, respectively; $D = [2b/(b+1)]D_p$ is the ambipolar diffusion coefficient, D_p is the hole diffusion coefficient, and $L = (D\tau_{ph})^{1/2}$. The voltage drop across the base, V_b, is given by:

$$V_b = \frac{j}{q(\mu_n+\mu_p)}\int_0^{W_n}\frac{dx}{p(x)+N_o} \tag{12}$$

$$p(x) = \frac{p_o \sinh\frac{W_n - x}{L} + p_W \sinh\frac{x}{L}}{\sinh\frac{W_n}{L}} \tag{13}$$

$$p_o = j\frac{b}{b+1}\cdot\frac{2L}{qD}\cdot\frac{1}{1+\sqrt{1+4jj_{ns}\frac{b}{b+1}\left(\frac{L}{qDn_i}\right)^2}} \tag{14}$$

$$p_W = j\frac{1}{b+1}\cdot\frac{2L}{qD}\cdot\frac{1}{1+\sqrt{1+4jj_{ns}\frac{1}{b+1}\left(\frac{L}{qDn_i}\right)^2}} \tag{15}$$

$$N_o = \frac{b}{b+1}\cdot n_o, \quad n_o = N_d.$$

where n_0 is free electron concentration in the base ($n_0 = N_d$); and W_n is the width of the i-region. The following values of 4H-SiC parameters are generally used at 300K: the electron to hole mobility ratio $b = 8$ ($\mu_n = 800$ cm^2/V·s, $\mu_p = 100$ cm^2/V·s), $D_p = 2.6$ cm^2/s, $n_i = 1.2\times10^{-8}$ cm^{-3}. As mentioned above, the leakage current j_s in 4H-SiC is as small as ~10^{-45} A/cm^2 at 300K. Moreover, j_s is severely dependent on temperature: in the

temperature range 300-600 K, j_s varies between ~10^{-45} and ~10^{-17} A/cm^2. It was suggested to introduce instead of j_s a new fitting parameter a:

$$\alpha = j_s\left(\frac{L}{qDn_i}\right)^2. \tag{16}$$

Within the temperature interval 300-600K a varies (1.5-2)-fold. Physical limitations on a can be established by comparing (7) and (16) with the standard expression for the emitter injection efficiency γ [11, 21]:

$$\gamma = \frac{j_p}{j_p + j_n} = \frac{1}{1+\frac{N_d}{N_a}\left(\frac{D_n\tau_p}{D_p\tau_n}\right)^{1/2}}. \tag{17}$$

where τ_p is a hole lifetime which can be different at low and high injection levels. Equation (17) is valid at $W_n >> L_p$ and $W_p >> L_n$. In the simplest case γ_{max} is assumed to be close to unity (since $N_a >> N_d$), and $\gamma_{min} = 1/2$ (symmetrical p-n structure). Using (7), (16), and (17) we obtain:

$$\gamma = \frac{1}{1+\alpha q N_d\left(\frac{2b}{b+1}\right)^{1/2}\left(\frac{D_p}{\tau_p}\right)^{1/2}} \quad \text{for the condition:} \tag{18}$$

$$0 < \alpha < \left[qN_d\left(\frac{2b}{b+1}\right)^{1/2}\left(\frac{D_p}{\tau_p}\right)^{1/2}\right]^{-1}.$$

By using (16), we can simplify (11), (14), and (15):

$$j_o = \frac{qDn_i}{2L}\cdot\frac{b+1}{\sqrt{b}}\left[\left(1+\sqrt{1+4j\frac{\alpha b}{b+1}}\right)\cdot\left(1+\sqrt{1+4j\frac{\alpha}{b+1}}\right)\right]^{1/2} \tag{19}$$

$$p_o = j\frac{b}{b+1}\cdot\frac{2L}{qD}\cdot\frac{1}{1+\sqrt{1+4j\frac{\alpha b}{b+1}}} \tag{20}$$

$$p_W = j\frac{1}{b+1}\cdot\frac{2L}{qD}\cdot\frac{1}{1+\sqrt{1+4j\frac{\alpha}{b+1}}}. \tag{21}$$

This model has been shown to effectively model 5.5 kV 4H-SiC PiN rectifiers in [19] operation at superhigh current densities of up to 50,000 A/cm^2. Modeling up to such high current densities is an important subject for SiC power devices, because of an increasing military and commercial interest in pulsed power devices.

3. Experimental Results on PiN Rectifiers

3.1. *PiN rectifier structures measured*

The development of hot wall CVD reactors to obtain SiC epitaxial layers with high purity, low defect density, and with sufficiently high minority carrier lifetimes layers were crucial to the realization of PiN rectifiers with respectable blocking voltage while providing low on-state voltage drop. These reactors have enabled minority carrier lifetimes to a level that enables the realization of SiC rectifiers with <4.5 V on-state drop at 100 A/cm^2. Probably the first high voltage rectifiers with good performance were the 4.5 kV (width of the blocking n-base = 45 μm) [22] and the 3.4 kV (W=30 μm [23]) rectifiers.

The first successful attempt in the demonstration of a >5 kV 4H-SiC rectifier was done using a 4H-SiC n^- epitaxial layer with a thickness of 85 μm and a doping of 1 to 7 X 10^{14} cm^{-3} [24]. Other demonstrations [25, 26, 27] of >3 kV 4H-SiC PiN rectifiers show that extremely high switching speeds and an on-state voltage drop comparable to Si PiN rectifiers are achieved when operated at sufficiently high current densities. The highest voltage functional semiconductor device ever reported is the 19.3 kV SiC PiN rectifier [28]. After a long development process [30], the highest power single chip SiC device (a PiN rectifier) was demonstrated recently with a 7.4 kV, 330 A (pulsed) capability [31]. Similar devices have been put in active circuits to show the benefits of SiC PiN rectifiers for utility applications [32].

3.2. *PiN rectifier fabrication process*

Typically, the most critical part of the fabrication of PiN rectifiers is the implementation of the edge termination. PiN rectifiers Anodes usually have rounded edges to minimize concentration of electric field during their reverse bias operation. If this edge termination is implemented using ion implantation, the choice of implanted species is a critical decision. Whereas Aluminum offers higher and more precise activation than Boron because of its lower acceptor level, it's larger atomic size causes much more damage to the crystal lattice. If this damage is not annealed using suitable high temperature implant anneals, this damage may cause excessive leakage in large area SiC PiN rectifiers. For the mesa-JTE design (as shown in Figure 2), an optimum dose of Boron is implanted at >1000°C after reactive ion etching through the 2 μm p^+ Anode cap layer with more than 5x10^{18} cm^{-3} doping. The JTE dimension of 75 to 100 μm may be used for 5 kV devices, and 250 to 500 μm for 10 kV devices. The ion implant damage is usually annealed at >1600 °C under Si overpressure condition, followed by a 1-3 μm LTO SiO_2 deposition. Thereafter, backside ohmic contact may be formed using metals like Nickel and p-type ohmic contact metal like Titanium is deposited as Anode metal. These metals are annealed at temperatures in the 700 to 1000 °C range to form the PiN Anode and backside cathode contacts. These metals were followed by a thick 1-3 μm metal stack deposition (for example Ti/Pt/Au) to reduce the resistance and enable wire bonding. Devices are then diced, brazed and wire-bonded for further characterization.

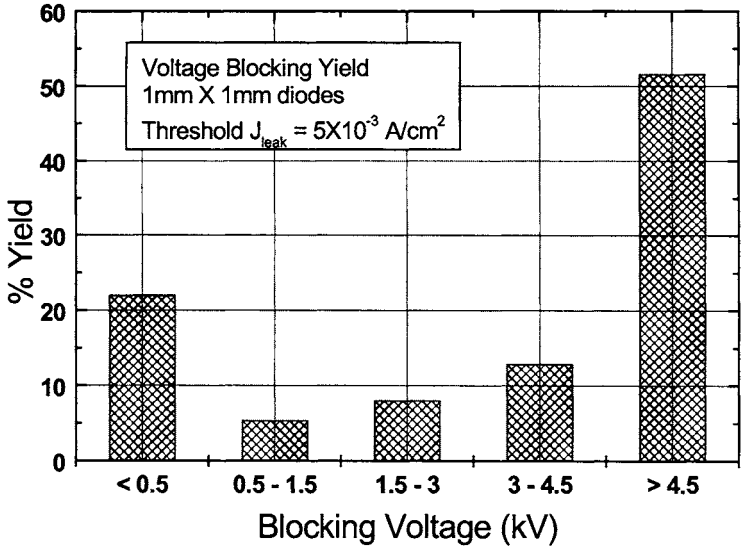

Figure 8: On-wafer yield of >50 % was obtained for 1 mm^2 rectifiers capable of blocking >4.5 kV for a leakage current density threshold of 5X10^{-3} A/cm^2.

3.3. *5 kV PiN Rectifiers*

At the time, the state-of-the-art characteristics of PiN rectifiers were given in ref [30]. In this report, a set of 1 mm^2 and 4 mm^2 rectifiers were designed for 5 kV operation using a 50 μm thick voltage blocking epitaxial layer with a doping of 9x10^{14} cm^{-3} on low micropipe density (<30 μP/cm^2) 4H-SiC n$^+$ substrates. The on-state voltage drop was usually uniform (i.e. ± 0.2 V) across the wafer and was not a yield-limiting factor. The mesa-JTE edge termination design outlined earlier and its associated processing allowed a yield of >50 % for 1 mm^2 rectifiers capable of blocking >4.5 kV when using a leakage current density threshold of 5X10^{-3} A/cm^2. The percentage distribution of all 1 mm^2 devices obtained from the wafer versus blocking voltage ranges is shown in Figure 8. As seen from this figure, 27 % of all devices block less than 1500 V, primarily due to materials defects such as micropipes. The reverse bias characteristics of a 2 mm X 2 mm rectifier are shown in Figure 9.

The measured leakage current density for these rectifiers was <10^{-3} A/cm^2 at 5 kV, and thereafter it increases dramatically at about 5.3 kV. The breakdown characteristics were not catastrophic; with the device surviving after the applied voltage was reduced. High temperature (up to 225 °C) measurements were performed only at 2 kV because of equipment limitations. The leakage current increases exponentially with temperature, but was still found to be less than 4x10^{-5} A/cm^2 at 225 °C at 2 kV for a 4 mm^2 rectifier, as shown in Figure 10. In standard commercial Si power devices, a leakage current density of <10^{-2} A/cm^2 is considered acceptable for defining blocking voltage. These results show that the edge termination design adopted for these devices is quite robust even at high temperatures.

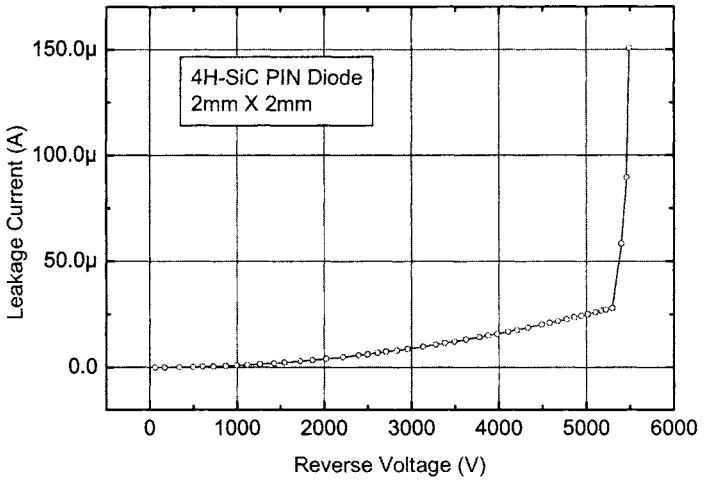

Figure 9: Blocking characteristics of a 5.3 kV rectifier capable of carrying >20 A.

The forward I-V characteristics show that at a high current density of 1250 A/cm^2 (50 Amperes on a 2 mm X 2 mm device), the on-state voltage drop was only 6.9 V, which was significantly affected by the wire bonding resistance. The measured temperature dependence of the on-state characteristics for a 5 kV SiC PiN rectifier device with a

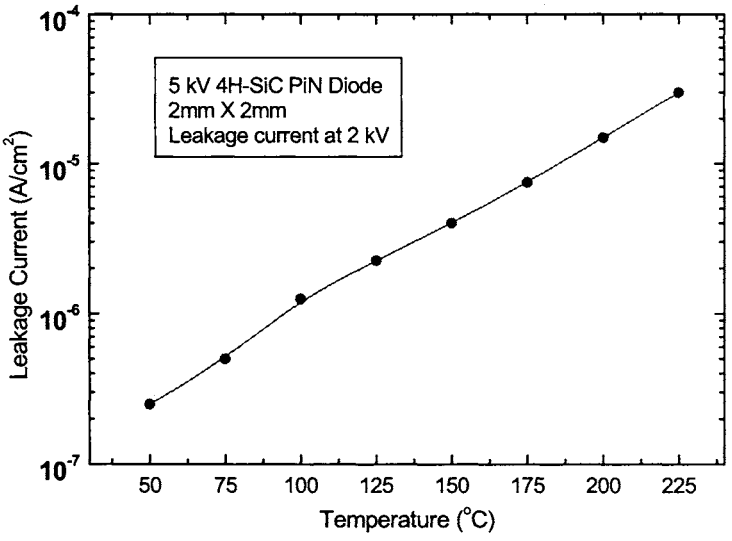

Figure 10: The leakage current density was less than 4x10^{-5} A/cm^2 at 225 °C at 2 kV for a 0.04 cm^2 rectifier, even after an exponential increase with temperature.

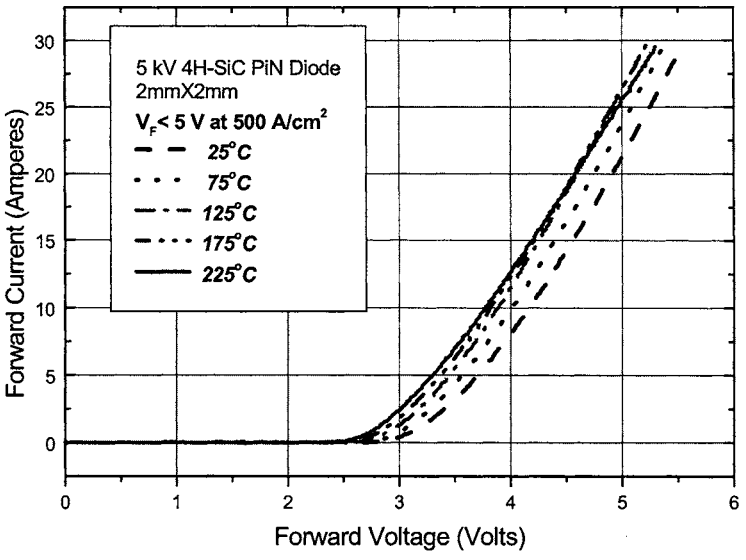

Figure 11: The measured temperature dependence of on-state characteristics.

typical current of 20 A (4 mm^2), is shown in Figure 11. The decrease in on-state voltage with temperature is indicative of the increase in lifetime with increasing temperature for a conductivity modulated device and a decrease in bandgap of the PN junction. However, at a high temperature of 225 °C, a reduction in carrier mobility starts to increase the differential on-resistance across the i-layer. This leads to a cross-over in the I-V characteristics at a high current density of 500 A/cm^2. In the entire 25 °C to 225 °C range, the change in on-state voltage drop remains in a somewhat insignificant 0.4 V range, as seen from Figure 11. This shows that SiC PiN rectifiers are stable with temperature. In case of Si rectifiers, over 40% reduction in on-state voltage drop was measured in the 25°C to 125°C range [8]. This results in poor current sharing when such devices are operated in parallel because of the generation of 'hot spots' that hog a large amount of current.

Detailed switching measurements were also conducted on some 5 kV blocking 4H-SiC PiN rectifiers. The most important dynamic characteristics for a rectifier are its reverse recovery characteristics, and their variation with operating temperature. The reverse recovery tests were performed for various values of di/dt. Figure 12 shows the current vs. time waveforms of the 20 A, 5 kV SiC PiN rectifiers for three different reverse di/dt values. At the conventional 40 A/μsec, the peak reverse current was only 65 % of the forward current. As the reverse di/dt was increased to 100 A/μsec and 1700 A/μsec, the peak reverse current to forward current ratio increased to 90 % and 150 %, respectively. As compared to high voltage Si PiN rectifiers, this is a relatively insignificant change, considering that extremely high reverse di/dt values were used. This effect could be explained by the fact that the amount of reverse recovery charge in SiC rectifiers is at least 3 orders of magnitude smaller than Si rectifiers.

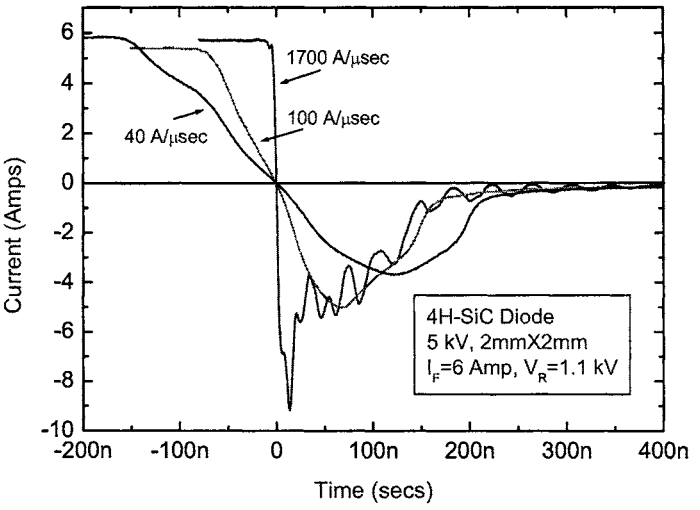

Figure 12: Reverse recovery characteristics show a 2X increase in the peak reverse recovery current when the reverse di/dt was increased from 40 A/μsec to an extremely high 1700 A/μsec.

The temperature dependence of the rectifier switching characteristics for a 2 mm X 2 mm 5 kV device is shown in Figure 13. These measurements are taken at a relatively high reverse di/dt of 175 A/μsec, when the rectifier is switching near zero voltage at 6.2 A. Usually, the reverse bias applied does not affect the reverse recovery characteristics. As seen from this figure, the peak reverse current increases by a modest 50% when the

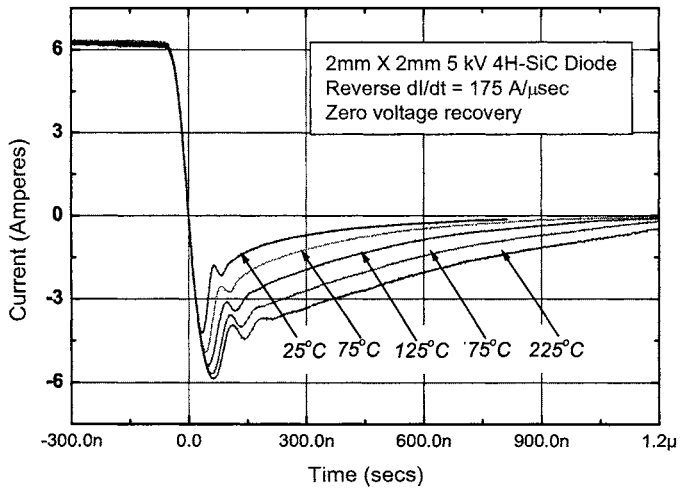

Figure 13: High temperature reverse recovery characteristics show a modest increase in the peak reverse current as the operating temperature is increased from 25 °C to 225 °C.

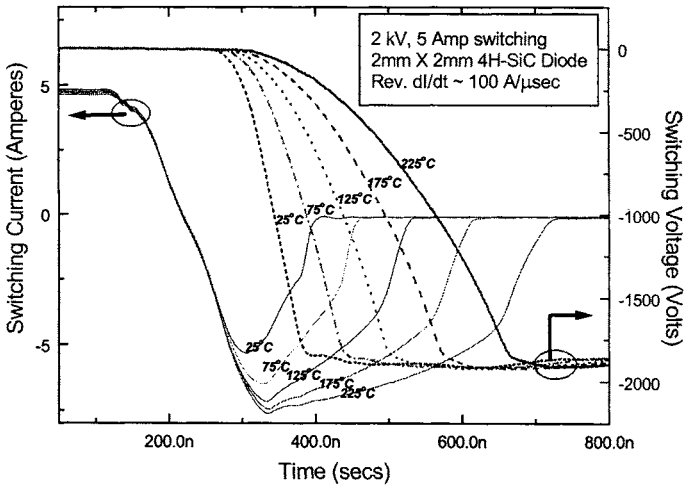

Figure 14: Current and voltage waveforms of a 5 kV rectifier switched at 25 °C, 75 °C, 125 °C, 175 °C and 225 °C.

temperature was increased from 25 °C to 225 °C. The total reverse recovery charge, which is the area under the I-t curve when the rectifier is undergoing reverse recovery, increases by approximately 100 %, as the operating temperature is increased from 25 °C to 225 °C. These rectifiers show repeatable switching characteristics as the operating temperature was increased from 25 °C to 225 °C. The turn-off time increases from 0.2 μsec to 0.65 μsec while switching 125 A/cm^2 (5 A) and 2 kV with a reverse di/dt of 100 A/μsec, as shown in Figure 14. A level of 2 kV was chosen as the highest voltage possible for the pulse generator used in this measurement. These rectifiers do not show a "snappy" recovery and have substantially smaller noise signatures when compared to 600 V Silicon PiN rectifiers.

Figure 15 shows that the on-state voltage drop changes from 3.9 V to 3.4 V at 150 A/cm^2 as the operating temperature is increased from 25 °C to 225 °C. Under the same conditions, the measured reverse recovery charge increases from $0.5X10^{-6}$ C to $1.3X10^{-6}$ C. This is a 10^3X reduction in Q_{rr} as compared to comparably rated Si (in terms of blocking voltage) rectifiers. It is worthwhile to note that reverse recovery charge shows a 4-6X increase with temperature from 25°C to 125°C, even for ultrafast Si rectifiers [33]. Two factors contribute to the dramatically smaller reverse recovery charge (Q_{rr}) in 4H-SiC rectifiers as compared to similarly rated Si rectifiers: (a) the 20-25X thinner voltage blocking layers with 20X higher doping dramatically reduce the total volume of excess charge in the i-layer and (b) the carrier lifetime required for these thinner voltage blocking layers can be >10X smaller than those required for Si devices for a similar i-region voltage drop. A much smaller carrier lifetime and thinner voltage blocking layer in 4H-SiC results in a very stable on-state voltage drop with temperature.

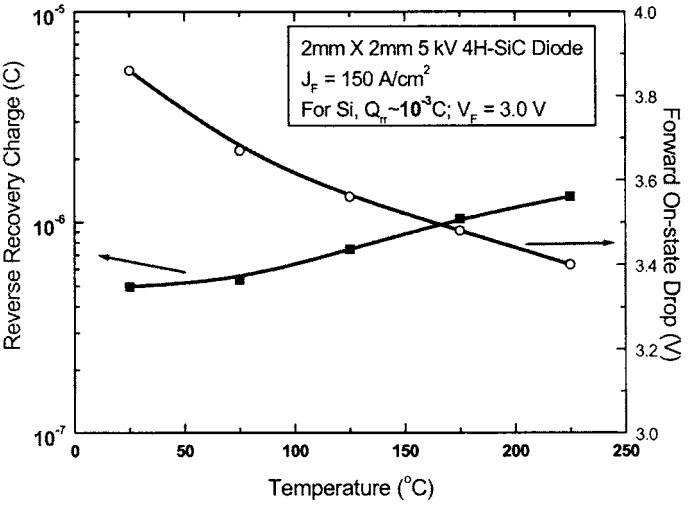

Figure 15: Reverse recovery charge and on-state voltage drop as a function of temperature for a 5 kV PiN rectifier.

3.4. *9mm^2, 10 kV 4H-SiC PiN Rectifiers*

Another set of PiN rectifiers were designed for 10 kV blocking with an active area of 9 mm^2 using a 150 μm thick voltage blocking epitaxial layer with a doping of 1 to 3x10^{14} cm^{-3}. Data obtained on these 4H-SiC PiN Rectifiers shows a very uniform on-state voltage drop across the wafers. At 2 kA/cm^2, the differential on-resistance was only 3 mΩ-cm^2, as shown in Figure 16. The reverse bias characteristics of a 3 mm X 3 mm rectifier are shown in Figure 17.

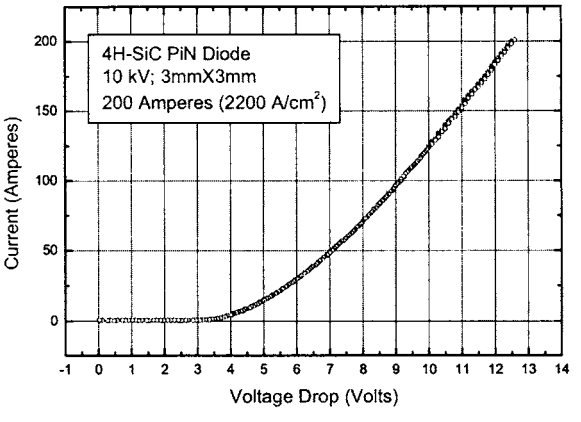

Figure 16: Pulsed (250 μsec) on-state characteristics of a 4H-SiC PiN rectifier capable of blocking 10 kV.

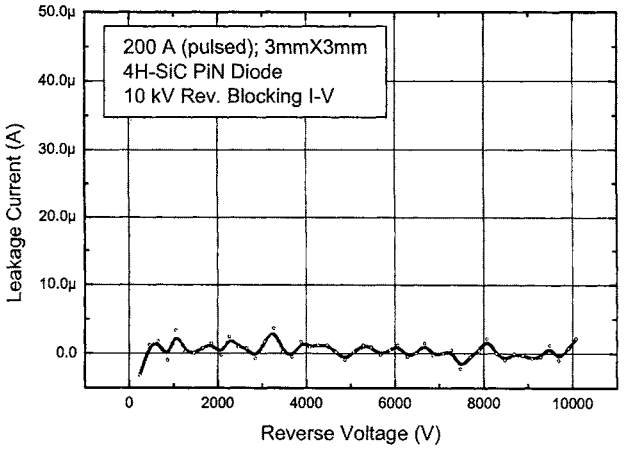

Figure 17: Blocking characteristics of a 10 kV rectifier capable of carrying >200 A (pulsed).

The measured leakage current density was $<10^{-4}$ A/cm^2 at 10 kV and increases dramatically thereafter. The device survived after the voltage was reduced, and then re-applied. High temperature (up to 200 °C) measurements on 8 kV capable packaged devices fabricated alongside the 10 kV rectifier shows that the leakage current increases with voltage beyond 150 °C, resulting in a blocking voltage of about 5.3 kV at the leakage current threshold of 20 µA, as shown in Figure 18. The choice of this leakage current is quite arbitrary, and was limited by the highest leakage current capability of the measurement equipment.

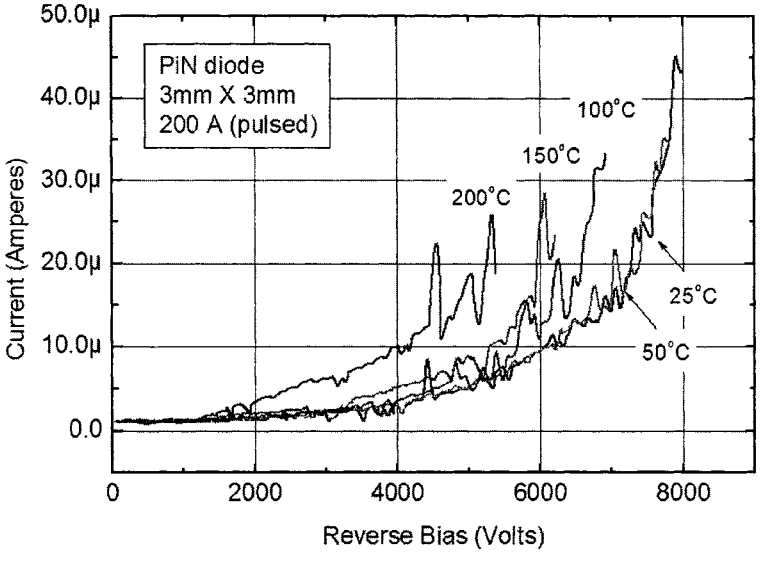

Figure 18: Reverse I-V characteristics of a packaged 8 kV PiN rectifier fabricated alongside the 10 kV blocking rectifier.

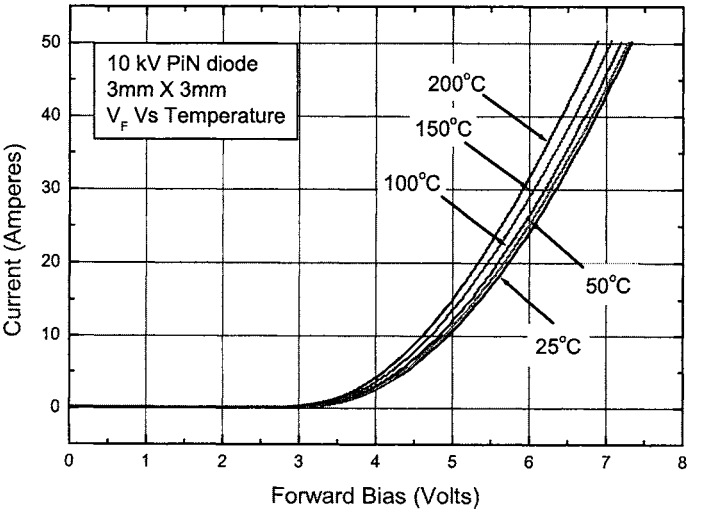

Figure 19: Forward I-V characteristics of a packaged 8 kV PiN rectifier fabricated alongside the 10 kV blocking rectifier.

The measured temperature dependence of the on-state characteristics for a 10 kV, 9 mm^2 SiC PiN rectifier is shown in Figure 19. The decrease in on-state voltage with temperature is indicative of the increase in lifetime with temperature for a conductivity modulated device, and a decrease in bandgap of the PN junction. However, at a high temperature of 200°C, a reduction in carrier mobility starts to increase the differential on-resistance across the i-layer (data not shown here). In the entire 25 °C to 200 °C range,

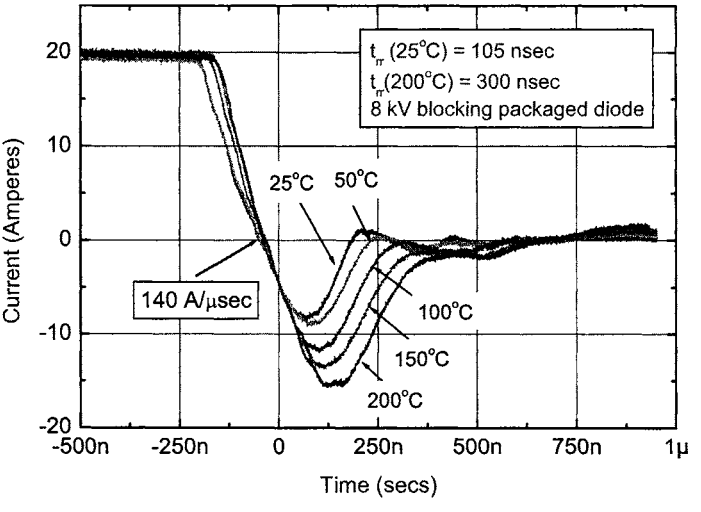

Figure 20: High temperature reverse recovery characteristics show a modest increase in the peak reverse current as the operating temperature is increased from 25 °C to 200 °C.

the change in the on-state voltage drop remains in a somewhat insignificant 0.4 V range.

Detailed switching measurements were conducted on some 8 kV blocking 4H-SiC PiN rectifiers fabricated alongside the 10 kV rectifiers. The temperature dependence of the rectifier switching characteristics for a 3 mm X 3 mm 10 kV device is shown in Figure 20. These measurements are taken at a relatively high reverse di/dt of 142 A/μsec, when the rectifier is switching from an on-current of 20 A to a blocking voltage of 600 V. As seen from this figure, the peak reverse current increases by a modest 110 % when the temperature was increased from 25 °C to 200 °C. The total reverse recovery charge, which is the area under the I-t curve when the rectifier is undergoing reverse recovery, increases by approximately 100 %, as the operating temperature is increased in this temperature range. These rectifiers show fairly stable switching characteristics as the operating temperature was increased from 25 °C to 200 °C. The turn-off time increases from 0.2 μsec to 0.7 μsec while switching 220 A/cm^2 (20 A). It is very encouraging to note that the total reverse recovery charge increases from an insignificant 1.17 μC to 3.8 μC as the temperature was increased from room temperature to 200°C. These rectifiers do not show a "snappy" recovery and have substantially smaller noise signatures when compared to Silicon PiN rectifiers.

4. Yield and Reliability of SiC Rectifiers

4.1. *Yield limiting factors in SiC rectifiers*

Usually, fairly uniform on-state characteristics are obtained across the wafers since the advent of hot-wall epitaxial reactors, and good anode ohmic metal processing. However, the yield due to blocking voltage on 4H-SiC devices is dependent on many material, processing and design related issues. Material related issues include: micropipes on the wafers, epitaxial growth related defects, and crystal defects like dislocations and stacking faults. It is difficult to quantize the effect of each of these factors on device yields, but great deal of data on these effects have been studied in reference [34]. Processing related issues are related to ion implant activation of JTE termination species, uniformity of the mesa etch, and quality of the dielectric used in passivation of edges. Design related effects on yield are junction edge diameter, and the choice of dose for JTE implanted species. As mentioned earlier, it is very difficult to separate the influence of all these parameters on device yields. Assuming a random distribution of defects, device yield is given by

$$Y = e^{-A.d} \tag{22}$$

where Y is the yield, A is the area (in cm^{-2}) of the device and 'd' is the defect density in cm^{-2}. Many researchers propose that the biggest yield-limiting factor in modern high voltage devices is micropipes. Figure 21 shows yield as a function of device current levels (assuming 100 A/cm^2) for different defect densities according to equation 22. As shown in an earlier section on the experimental results of PiN rectifiers, the yield on 1 mm^2 rectifiers was 52% at 4.5 kV. For 4 mm^2 devices, the obtained yield was approximately 20% at >4.5 kV; and for 9 mm^2 it was 22% at >7 kV. All these devices show quite abrupt breakdown characteristics at room temperature.

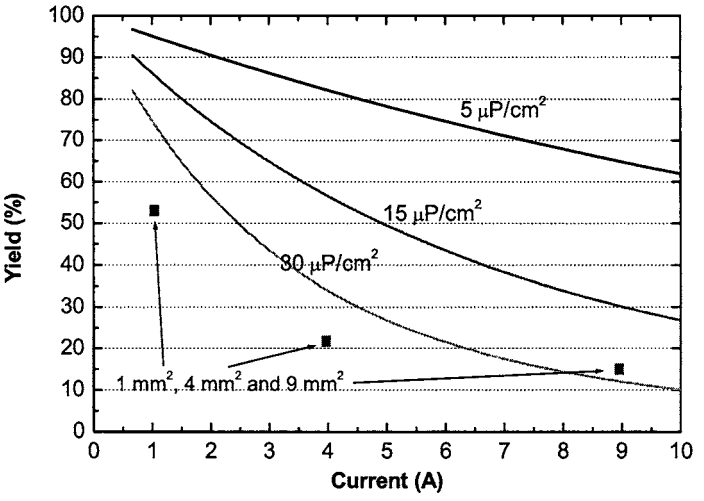

Figure 21: Theoretical and experimentally obtained yields on 1 mm², 4 mm² and 9 mm² devices at 4.5 kV, 4.5 kV and 7 kV.

All these devices were fabricated using similar processing techniques. However, the 9 mm² devices were fabricated roughly 18 months after the 1 mm² and 4 mm² devices, and might have benefited from an improvement in micropipe densities realized with time.

4.2. *Forward voltage degradation in SiC PN rectifiers*

While the reverse bias operation of SiC devices have been found to be relatively stable if good edge termination and passivation techniques are used, a curious

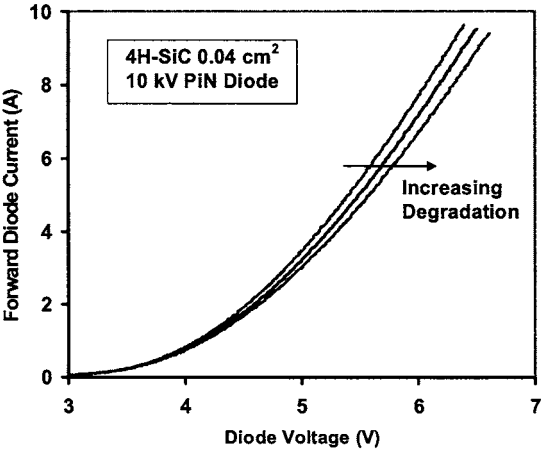

Figure 22: On-state characteristics of a high voltage SiC PiN rectifiers after various levels of forward bias stress.

phenomenon observed during the forward bias operation of SiC PiN rectifiers has caused a great deal of concern towards long term stability and reliability of these devices. It has been observed that as PN rectifiers are forward biased for an appreciable length of time, their on-state voltage drop increased with time, as shown in Figure 22. The duration over which these devices show this forward bias degradation varies from a few milliseconds to many hours [35]. A variation in on-state voltage drop (V_F) in PiN rectifiers has serious stability concerns because it can result in current filamentation and local current 'hogging'. If a portion of the rectifier has a lower on-state voltage drop than another region within the same rectifier, current will be diverted into the lower V_F region. This can cause excessive current densities in small portions of the rectifier, while leaving large portions of it with a low current density, leading to thermal instability of the entire rectifier. Such a situation will also prevent safe paralleling of devices to boost the total current required for typical high current applications for which these devices are targeted.

Optical observation of PN rectifiers undergoing VF degradation shows a concomitant formation of a certain material defect in these rectifiers, as shown in Figure 23. Probably the first report of this phenomenon, which were termed as 'Bright line defects', was made by Konstantinov et al [36], since they appear are mobile bright lines. This was compared to the previously studied formation of 'Dark line defects' in Gallium Arsenide light emitting devices [37], where dislocation growth due to non-equilibrium carrier injection and crystal strain results in a similar forward bias degradation phenomenon. Many researchers agree that mobile and propagating crystal stacking faults are the primary cause of forward bias degradation of PN rectifiers. This defect propagates through the entire n- base layer. It was initially proposed [38] that the increase in V_F is caused by reduced carrier lifetimes due to the formation of recombination centers from stacking faults. However, more recent results indicate that the increase in V_F causes the stacking faults to form a barrier to current flow and reduce the conduction area. A stacking fault defect is a two-dimensional error in the atomic stacking sequence of a polytype of SiC.

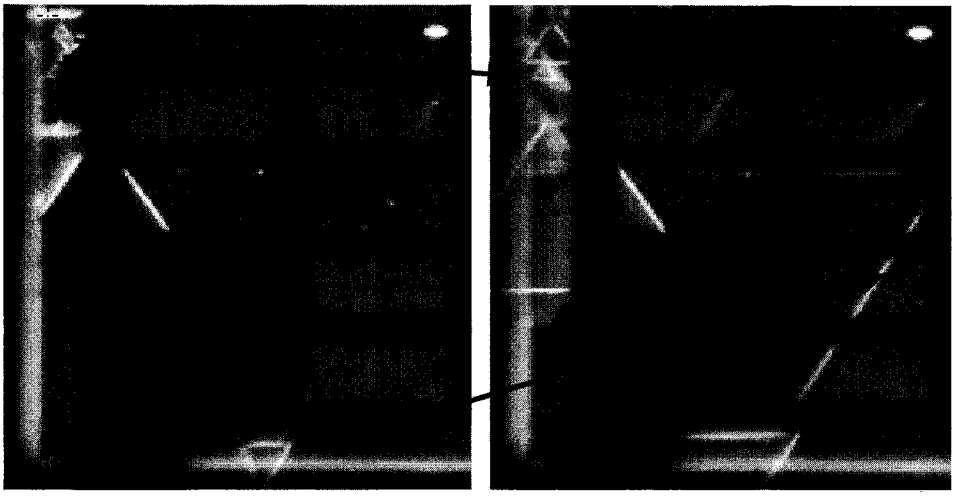

Figure 23: Light emission measurements of a PiN rectifier before (left) and after (right) forward bias stress indicating growth of stacking faults.

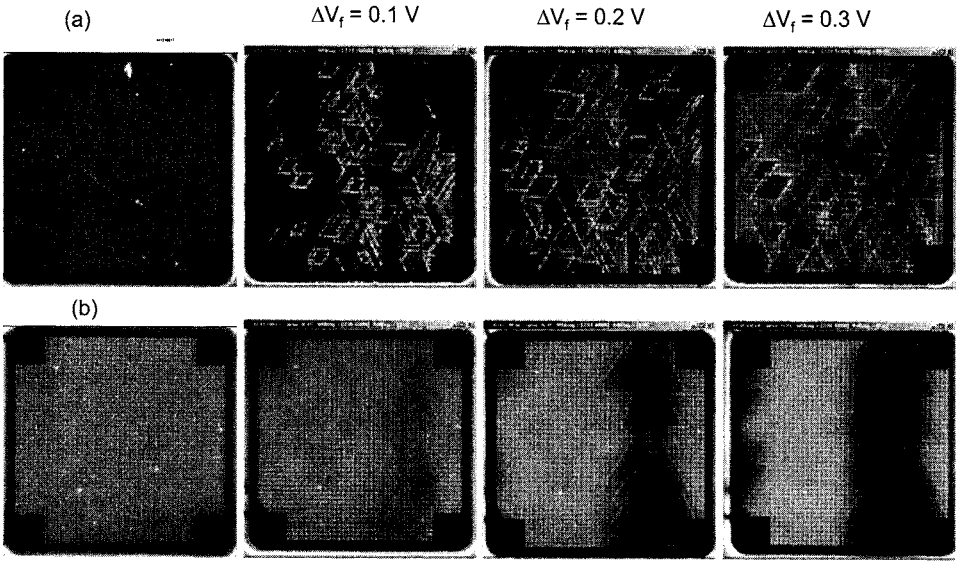

Figure 24: Light emission images at various intervals during degradation for two adjacent rectifiers (a) top and (b) bottom on the same chip.

Figure 24 shows a series of light emission images at various intervals during degradation for two adjacent 0.015 cm^2 rectifiers on the same chip. These optical phenomena were correlated with a lifetime measurement method that uses the turn-off reverse-recovery waveforms for conditions of high dI/dt and low dV/dt [39]. This result indicates that the effective i-region lifetime is not reduced and the V_F degradation is due to a reduction in conduction area. Figure 25 (a) and (b) show the forward bias voltage degradation and reverse recovery current for the same rectifiers as those shown in Figure 23 and Figure 24, where the arrows on Figure 25 (a) and (b) indicate the time for each frame in Figure 24 (a) and (b), respectively. The rhomboid shaped regions in Figure 24 (a) indicate stacking faults emanating from near the surface, presumably from the P-N junction. It is determined that these stacking faults are near the surface by the growth direction and shape as well as by changing of the focal plane of the CCD camera. The device degrades rapidly in Figure 25 (a) because the highest excess carrier concentration is near the P-N junction. The outlined triangular dark regions in Figure 24 (b) indicate stacking faults growing from near the n^+/n^- junction. The white outlines are from partial dislocations that bound the stacking faults and the dark regions indicate regions where current is reduced. The device degrades more slowly at first, as can be seen in Figure 25 (b), because the stacking faults are near the bottom of the i-layer where the excess carrier concentration is lower and the degradation rate increases as the stacking faults approach the P-N junction at the surface where the excess carrier concentration is larger.

The fundamental nature, origin and propagation of these dislocations have been extensively investigated by various researchers [38, 40, 41]. It is now established that these defects nucleate from existing substrate crystal defects in hexagonal (eg. 4H and 6H) SiC. The hexagonal crystal structures of these polytypes of SiC are formed when three distinct atomic patterns are stacked in a particular sequence. This is in contrast with cubic (3C) SiC, which has a fundamentally two dimensional structure with only two

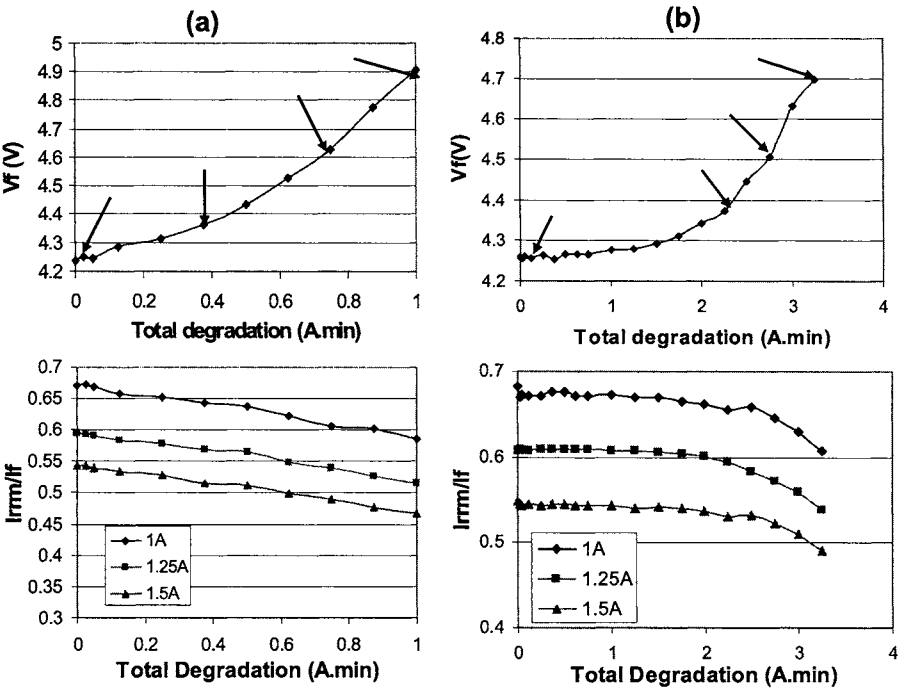

Figure 25: The on-state voltage VF (at 100 A/cm^2) degradation and reverse recovery current for the same rectifiers in Figure 24 (a) and (b), respectively.

atomic patterns stacked together. Hence, 4H-SiC and 6H-SiC crystals are metastable at room temperature and could convert to a locally faulted 3C-like structure if an appropriate nucleating site was present [42]. For this to occur, a proper type and density of nucleation sites and the activation energy in the form of electron-hole pair recombination energy are needed. The control of the origin and propagation of these defects may lie in the control of pre-existing defects serving as nucleation sites for these defects.

Spectral analysis of the electroluminescence shows that these bright line defects emit light in the red and near-infrared spectral regions, in contrast to near-bandgap luminescence of non-degraded PN rectifiers which is predominantly in the violet region [40]. These defects were determined to be an irreversible formation of a network of linear defects related to crystal dislocations that subsequently propagate through, and then beyond the rectifier area. The nucleating sites for these stacking faults appear to be primarily at low angle grain boundaries, among other substrate and surface defects. The resulting stacking faults have been observed to be bound by Schockley partial dislocations with a Burger's vector b=1/3<10-10> [41]. This implies that the faults propagate as triangular or rhombohedral structures with edges along the 11-20 directions. These looping structures multiply and propagate as the rectifier is kept in the forward bias state. Spectral measurements show that the stacking faults have a primary emission spectrum in the 450 +/-20nm peak range [40], and those of threading dislocations is in the 700 +/-20 nm range. The calculated activation energy for the gliding (propagation) of

the partial dislocation that bounds the stacking fault is measured to be in the 0.27 +/- 0.02 eV range. In this experiment, it was estimated that the velocity of propagation of these defects was $7X10^{-5}$ m/s.

An activation energy of 0.27eV is small enough that most nucleating sites will result in the formation of these faults, and hence some degradation in the on-state voltage drop of PiN rectifiers. Hence, the solution for solving this problem lies in minimizing the defects in the active portion of the device. A novel approach to achieving this was recently demonstrated by growing of Lely crystals with no micropipes and only minimal defects on top of standard substrates [43]. In this experiment, an application of 200 A/cm^2 stress in the forward direction did not produce any degradation, which was observed with PN junction rectifiers using normal substrates. Recently, great strides have been made in 4H-SiC epitaxy to produce relatively drift-free PiN structures by reducing the material defect density [44]. From these preliminary results, it seems that reduction of material defects would be directly correlated to obtaining a high yield of drift-free PiN rectifiers in SiC.

Recently, various methods have been investigated for improving the V_F degradation [45]. The different methods produce different yields of degradation free devices with some processes having yields as high as 86% degradation free. In each degradation free process, some devices do not drift at all, while others drift a small amount and then stabilize. However, some of the processes also reduce the breakdown voltage yield. Most recently, a new Low basal plane dislocation (BPD) process demonstrates substantial increase in the overall yield with blocking and drift yields of 35% and 67%, respectively [46]. Figure 26 and Figure 27 show the degradation and monitoring results for a typical low degradation rate 50 A, 10 kV 4H-SiC PiN rectifier made with this process.

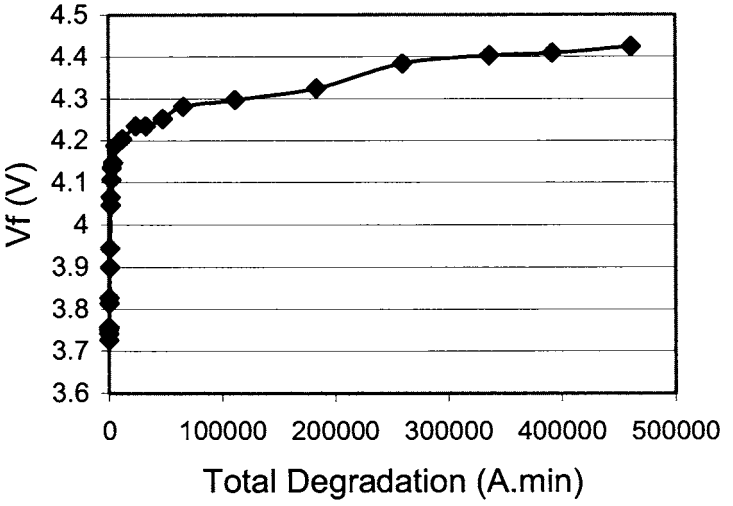

Figure 26: On-voltage voltage drop, V_F (at 50 A/cm^2) degradation as a function of total degradation for a 0.5 cm^2, 10 kV 4H-SiC PiN rectifier stressed at 50 A.

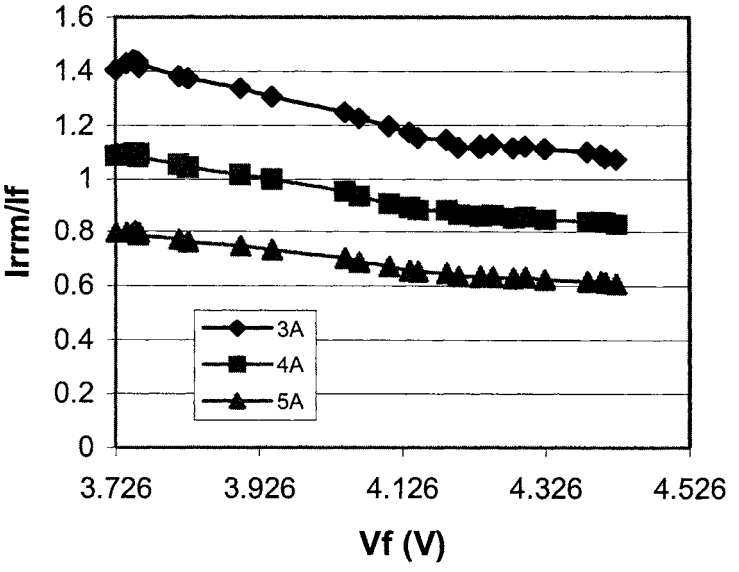

Figure 27: Reverse recovery peak as a function of total degradation for a 0.5 cm^2, 10 kV 4H-SiC PiN rectifier.

It is worthwhile to note that such a phenomenon is not observed in unipolar devices like Schottky rectifiers, even when the power density (on-current X V_F) approaches near levels at which the PN rectifiers show this phenomenon [47]. While detailed published reports are missing, anecdotal data suggests that the forward bias degradation associated with stacking faults occurs in bipolar SiC devices like Thyristors, GTOs, PiN rectifiers, and even bipolar junction transistors (BJTs), but is not observed in unipolar switches like MOSFETs and JFETs. The incidence of propagation of these dislocations was found to increase with higher current densities. Higher temperatures and thicker epitaxial thicknesses also resulted in a higher incidence of formation of dislocations. Probe scratches, chip scribe lines and even silicided contacts on PN rectifiers are considered to be nucleation sites for mobile and expanding dislocations.

5. Conclusions

Currently, there are significant efforts underway to accelerate the development and application insertion of new high voltage/high frequency SiC power devices including PiN rectifiers. These are needed for commercial and military power conversion and distribution applications. PiN rectifiers and switches are an enabling technology for alternative energy sources and storage systems. The emergence of such devices presents unique opportunities and challenges to the power electronics industry in specifying the device requirements and establishing pulse width modulation (PWM) converter topologies for high voltage applications. Rapid progress is continuing in the realization of ultra high voltage, high frequency PiN rectifiers with high yield and good reliability.

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