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Reliability of SiC MOS devices ☆

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Abstract

Fundamental limitations to oxide reliability are analyzed in silicon carbide based devices. A barrier height primarily determined by band offsets between metal/SiC and the dielectric, and the electric field in the dielectric results in tunneling current into the dielectric, resulting in its degradation. Since band offsets for SiC to most dielectrics are smaller than those with respect to Si, a lower reliability is expected for SiC-dielectric based devices as compared to Si MOS devices. Other researchers have correlated interface states in the SiC–oxide as tunneling sites that increase gate leakage currents and influence the barrier to tunneling. Depending on the allowed maximum electric field in the gate oxide, there exists a trade-off between on-state resistance and SiC MOS reliability.

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1. Introduction

A natural oxide (SiO_2) for SiC was considered a significant advantage as compared to other compound semiconductor materials, since it enables the power MOSFET the ideal SiC switch for a wide variety of applications. However, some fundamental physics based issues and technological development issues have prevented the realization of the full potential of a MOS based SiC power device, despite the decade long research on such devices. The most serious physical challenge to the realization of high-reliability MOS based SiC devices is due to tunneling currents into the oxide layer.

2. Tunneling current

The gate oxide thickness in both Si and SiC power MOSFETs is in the 30–100 nm range. At a typical gate bias of +10 to +30 V, MOS based devices typically have an oxide field in the range of 4–6 MV/cm. It is desirable to limit the tunneling current because tunneling currents generate defects in the oxide leading to their eventual degradation. The most commonly cited intrinsic oxide degradation mechanism in SiC is the Fowler–Nordheim (FN) tunneling [1–4], even though FN current is observed in Si based MOS device only beyond the 6 MV/cm range. For this tunneling mechanism, the electric field in the dielectric results in an emission of carriers from the semiconductor into the dielectric, or from the metal to the dielectric, resulting in time-dependent dielectric breakdown (TDDB). The tunneling emission current is of the form [5]:

$$J^0_{\text{F–N}} = A \cdot E^2 \exp\left(-\frac{B}{E}\right)$$

where $J^0_{\text{F–N}}$ is the tunneling emission current, E is the electric field in the dielectric, and A and B are dependent on the band offset of the relevant junction. The barrier

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height (Φ_B) is defined as the difference between the electron affinities of the metal/semiconductor and the dielectric. A and B have the following dependence on barrier height:

$$A \propto \frac{1}{\Phi_B}$$

$$B \propto (\Phi_B)^{3/2}$$

Note that tunneling current emission is exponentially dependent on both the electric field in the dielectric and the barrier height between the dielectric and the metal or semiconductor. The temperature dependence of FN tunneling is treated in detail by Pananakakis et al. [5]. To the first order, the FN current can be assumed to be proportional to the square of temperature, if the temperature dependence of Fermi level (and hence the barrier height) is ignored.

3. MOS under inversion

For this discussion, MOS under inversion is defined to be when an NMOS device has a positive bias on the gate with respect to the substrate, or when a PMOS device has a negative gate bias with respect to the substrate. Here, the discussion is concentrated on the NMOS case, while a similar parallel exists for the PMOS case. The barrier height for the purposes of FN tunneling is calculated as the difference between the conduction band of the dielectric and the Fermi level of the semiconductor. In the worst case scenario for an NMOSFET, the Fermi level may assumed to lie at the conduction band, which corresponds to a very strong inversion case, or when highly doped N-type SiC is used. For this condition, the barrier height for FN tunneling is the conduction band offset between SiC and the dielectric, which is SiO_2 for further discussion. FN tunneling currents are expected to be much higher for a SiC based MOSFET than for a Si based device for the same electric field because the conduction band offset between SiC and SiO_2 is smaller than that between Si and SiO_2. As shown in Fig. 1, the conduction band offset in the Si–SiO_2 interface is 3.2 eV, but it is only 2.7 eV for 4H–SiC. For the same FN tunneling current, this 0.5 eV difference in the band offset will require that the electric field in the dielectric for a 4H–SiC/SiO_2 system be reduced by approximately 1.5X as compared to a Si/SiO_2 system. In commercial Si NMOSFETs, the electric field in SiO_2 is kept below 4–5 MV/cm, so that a reasonable 10 yr life is achieved [6]. Tunneling is the primary device lifetime limiting factor for MOS based devices, and is rated only to a maximum temperature of 125 °C. For a 3 MV/cm maximum electric field in the dielectric of a SiC NMOS, the maximum gate bias must be limited to only +15 V for the typical 50 nm gate dielectric thickness at room temperature. At higher temperatures, the electric field in the dielectric (and hence the gate bias) must be made even smaller in order to make MOS reliability approach that of a Si MOS transistor. Although the valence band offset (and hence the barrier height) decreases more dramatically than the conduction band offset (from 4.7 eV in the Si/SiO_2 system to 3.05 eV in the 4H–SiC/SiO_2 system), PMOSFET reliability may be higher than NMOSFET reliability, because the band offset of 3.05 eV is still greater than the 2.7 eV for NMOS [7]. Ironically, the wider bandgap of SiC seems like a liability rather than an asset for high temperature operation because its band structure occupies a larger portion of the SiO_2 band structure.

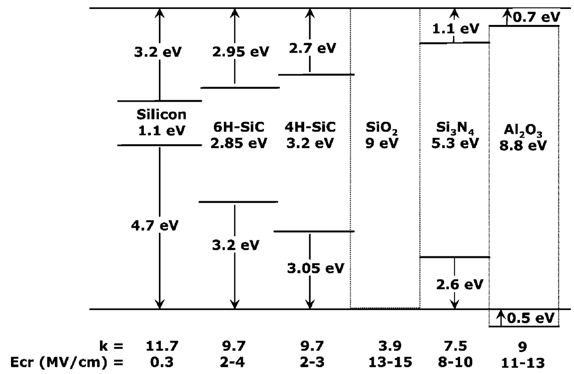

Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H–SiC, 4H–SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offsets of these are also shown with respect to SiO_2.

From this discussion, it seems that the reliability of a conventional SiC NMOS device is lower than that of a Si NMOS devices under typical operating conditions, and is unacceptably poor at higher operating temperatures. However, this conclusion is drawn from the worst-case scenario of assuming the barrier height for the purposes of FN tunneling is equal to the conduction band offset of 4H–SiC and SiO_2, i.e. the case of strong inversion. A significant gain in the barrier height may be achieved if the Fermi level in SiC is below the conduction band, i.e. an enhancement-mode MOSFETs (with p-type SiC) under weak inversion condition [8]. The gate bias range when the MOSFET is under a weak inversion condition is determined by the doping of the p-type base region. At the onset of weak inversion the barrier height (Φ_F) may be as much as 4.3 eV (1.6 + 2.7 eV, Φ_C), as shown in Fig. 2. A barrier height of 4.3 eV will allow a higher temperature operation of 4H–SiC based MOSFETs as compared to Si based MOSFETs (with a maximum barrier height of 3.75 eV), for an identical on-state electric field in the dielectric. This assumes that channel mobilities for Si and 4H–SiC MOSFET are similar for an identical electric field in the dielectric.

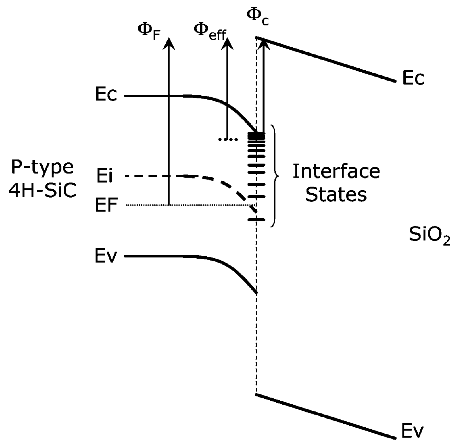

Fig. 2. Enhancement-mode SiC MOSFET under weak inversion case. The relevant barrier heights for FN tunneling in SiC–SiO_2 interface: Φ_C is the conduction band offset, Φ_F is the theoretical FN barrier height, and Φ_{eff} is the effective barrier height due to the presence of interface states at the SiC–SiO_2 interface.

Despite more than a decade of research, relatively modest success has been achieved in the realization of acceptable channel mobilities [9] for enhancement-mode NMOSFETs. Because of the low channel mobility observed in most 4H–SiC based MOS devices, a higher gate bias (and electric field) may be required in order to realize a low channel resistance in a SiC power MOSFET. This represents a challenge for achieving a high reliability in SiC based MOS devices at all temperatures. Hence, there exists an on-state performance/reliability trade-off determined by experimentally obtained channel mobility and the doping of the SiC used to make the NMOSFET.

4. Impact of interface states

The on-state/reliability trade-off is severely influenced by the experimentally obtained traps and carrier energy states at the SiC-dielectric interface. The origin of these traps is linked to the imperfect nature of 4H–SiC/dielectric interfaces, like the presence of carbon clusters [10] and/or dangling Si and C bonds. A significant number of electrons that are expected to provide the low on-resistance of the inversion layer get trapped in these energy states and scatter mobile electrons, further increasing the resistance in the channel region. Experimental data by Ouisse and Bano [11] shows that the low channel mobility in 4H–SiC is directly linked to extraordinarily high interface state densities in the SiO_2/SiC interface. In the energy band diagram, the interface traps that influence channel mobility are located between the Fermi level and the conduction band of the SiC, as shown in Fig. 2. Experimental data by Schorner [12] has shown that the density of these interface states exponentially increase beyond a level of 2.4 eV above the valence band of all SiC polytypes. This is used to explain the anomalously low electron inversion mobility in 4H–SiC MOSFETs, as compared to those obtained in other polytypes of SiC.

The location and density of interface states within the bandgap influences not only channel mobility, but also the FN tunneling currents at the SiC-dielectric interface. It has been shown [1] that the interface states act as the primary source of FN tunneling into the oxide, rather than the position of the Fermi level. Rather than a well defined barrier height determined by the difference between the Fermi level and conduction band, an 'effective' barrier height (Φ_{eff}) is typically observed in most cases which is determined by the density and location of the interface states [1] in the energy gap. Since most of the interface states are located close to the conduction band edge, Φ_{eff} is close to the conduction band offset of the SiC–SiO_2 interface. High temperature FN tunneling current data on n-type SiC by Li et al. [3] shows that the 'effective' barrier height decreases to only 2.38 eV as the operating temperature is increased to 300 °C as compared to the 2.7 eV conduction band offset difference at room temperature. Similarly, a lower FN tunneling barrier height was experimentally observed in 4H–SiC PMOSFETs by Chanana et al. [4], indicating the strong influence of interface states on FN tunneling current rather than the position of Fermi level.

It is sometimes mentioned that the low inversion layer mobility in power NMOSFETs may be acceptable for higher voltage (>2 kV) MOSFETs since a lower proportion of the resistance is contributed by the channel. However, if the MOS interface state density at the SiC-dielectric is high, the viability of these devices will be determined primarily by FN tunneling. The electric field in the dielectric must be kept correspondingly lower to limit FN tunneling current. The reduction in interface state densities in MOS structures will play a critical role in the on-state and high temperature performance, as well as reliability of power MOSFETs in 4H–SiC.

5. Conclusions

The reliability of SiO_2 in a SiC MOS based device is determined by tunneling current. If an intrinsic Fowler–Nordheim regime of tunneling is assumed, tunneling current is exponentially dependent on the electric field in the dielectric and barrier height to carriers. This barrier height is primarily determined by band offsets between metal/SiC and the dielectric. Since band offsets for SiC to most dielectrics are smaller than those with respect to Si, a lower reliability is expected for SiC-dielectric based devices as compared to MOS devices for the same oxide electric field. SiC-dielectric interface states affect channel mobilities and may determine the barrier height for Fowler–Nordheim tunneling. There exists a trade-off between on-state resistance and SiC-dielectric reliability, which is influenced by the dielectric thickness in a forward biased SiC-dielectric structure. The use of alternative dielectrics to improve this trade-off will soon be published in a detailed paper [13].

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