Application Note AN-10A: Driving SiC Junction Transistors (SJT) with Off-the-Shelf Silicon IGBT Gate Drivers: Single-Level Drive Concept

Introduction

GeneSiC Semiconductor is commercializing 1200 V and 1700 V SiC Junction Transistors (SJT) with current ratings ranging from 4 A to 16 A. SiC SJTs are normally-off, high-performance SiC switches, which are plug-in replacements for Si IGBTs. This document is the first of a two-part application note which will describe simple, yet optimized techniques for driving the SiC SJTs with a commercially available IGBT gate driver. This document describes a single-voltage level gate drive scheme, whereas a more optimized two-voltage level gate drive scheme for the SiC SJTs is described in GeneSiC document AN-10B.

SJT Gate Drive Circuit

A simplified gate drive schematic for driving the SJT, based on a single-voltage level concept is shown in Fig. 1. It features a commercial gate driver IC with an isolated input signal and a resistor-capacitor output network for improved switching performance.

In comparison to SiC MOSFETs, which require a non-standard +20 V gate bias due to poor transconductance characteristics, the SJTs can be driven with gate voltages as low as 8–10 V. The SJT also does not require a negative gate voltage to remain off.

The gate drive IC must be capable of supplying a continuous current of ~500 mA to the SJT gate during on-state operation. The external parallel gate resistor, R_{GP} should be adjusted to meet this requirement. As will be described in this document, the external parallel capacitor, C_{GP} can be appropriately chosen to ensure an optimum level of dynamic gate current during turn-on and turn-off initial transients. This dynamic current is essential for fast charging of the SJT's internal gate-source capacitance. The presence of this paralleled resistor and capacitor on the output of the gate driver can increase device switching speed, reduce device switching loss, and reduce driver losses as well. The selection of these component values is addressed later in this document.

While the IXYS IXDN614 gate driver [3] described in this document has shown to be capable of driving numerous SJT models without issue, several other commercially available driver options exist and may be employed for driving SiC SJTs. For the IXDN614, the output voltage V_O equals the supply voltage V_{GG} during the "high" output. Sufficient coupling capacitance (≥ 470 µF) should be added to the driver IC supply terminals to ensure consistent output power supply into the

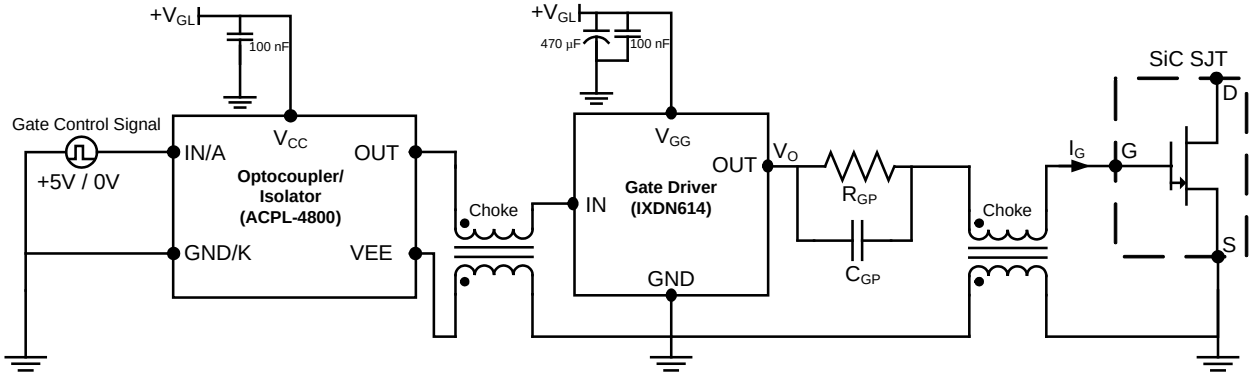

Figure 1 – SJT Single-Level Gate Drive Circuit

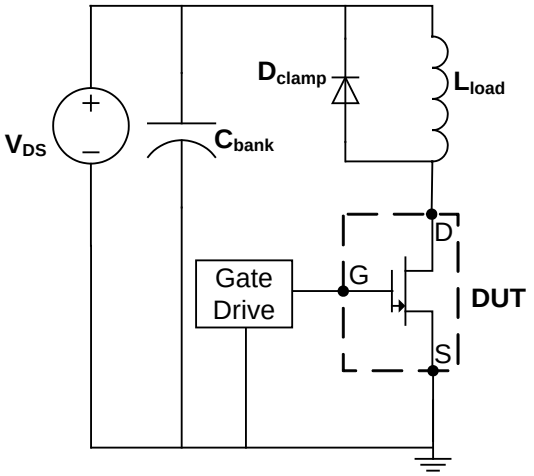

Figure 2 – Standard double pulse switching test circuit.

Table I – Double Pulse Example Testing Conditions

Parameter	Value
DUT	1200V / 6A SJT (GA06JT12)
D_{clamp}	1200V / 5A Schottky (GB05SLT12)
V_{DS}	600 V
I_D	6 A
V_{gg}*	15 V
R_{GP}*	22 Ω
C_{GP}*	18 nF
L_{load}	1.05 mH
T	25 °C

*- Denoted in Fig. 1

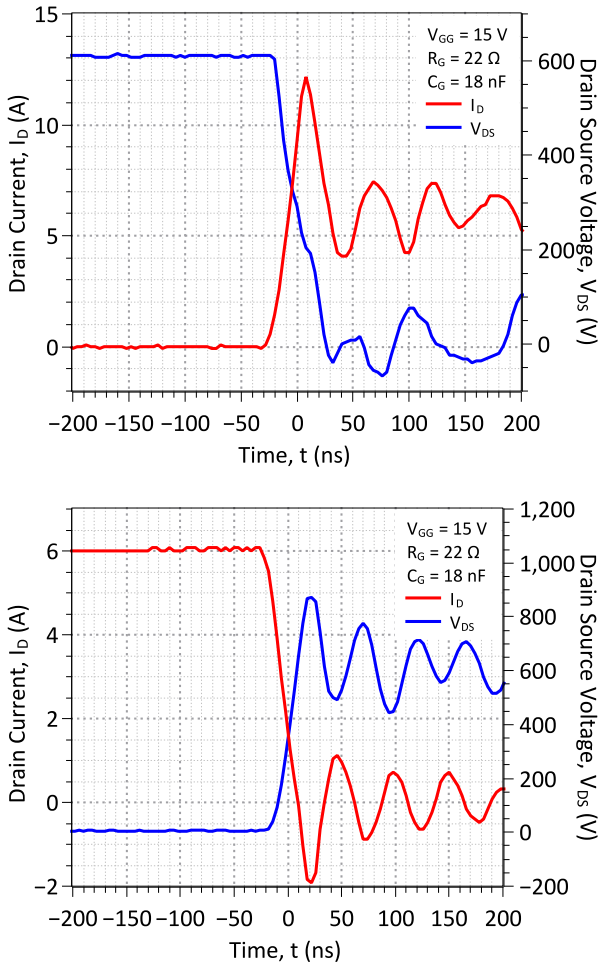

Figure 3 – Turn-on (top) and turn-off (bottom) switching waveforms of a 1200 V / 6 A SJT (GA06JT12-247).

SJT.

Due to the high voltage capability of SiC SJTs, an optocoupler or isolator should be used to protect the input signal source from potential high drain voltages. The isolation rating should greatly exceed the predicted DC voltages in use, particularly with an inductive load present. Also, choke coils are shown to be effective in reducing common-mode noise in the circuit on voltage supplies and gate driver inputs and outputs, they may be used when and where necessary.

SJT Switching Performance

An industry standard double-pulse switching test, shown in Fig. 2, has been performed to demonstrate SJT switching performance using the described gate drive circuit. During testing, the SJT is turned on with the application of a gate current I_G and the drain current I_D is ramped up linearly while flowing through the inductor and SJT in series until I_D = 6 A when the SJT is switched off. The device is then switched back on after a 2 µs delay to record device turn-on. Voltage and current waveforms of the SJT are shown in Fig. 3 of both SJT turn-on and turn-off [5].

Given the test conditions in Table I and utilizing the Fig. 1 gate driver, the SJT has a drain current rise time t_r of only 16 ns and a fall time t_f of 26 ns. The total device switching energy loss is only 97 µJ per cycle, equating to less than 10 W of device switching loss at 100 kHz. The SJT can be switched faster or with lower losses based on the values of R_{GP} and C_{GP}, these changes are detailed in the following section.

Gate Drive Parameter Selection

Driving an SJT is simple and nearly identical to driving a Si IGBT, as described previously. The

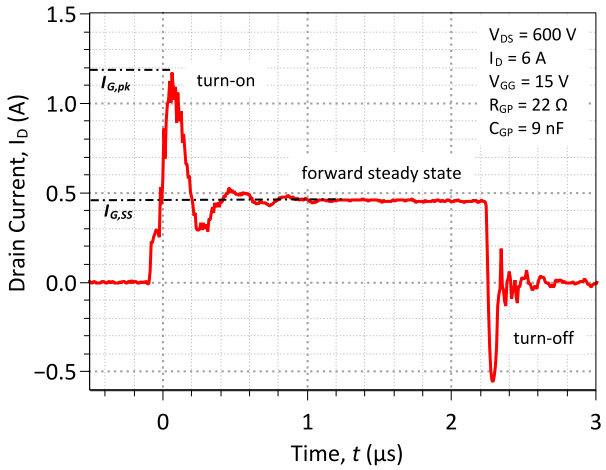

Figure 4 – Transient gate current I_G waveform while driving a 1200 V / 6 A SJT.

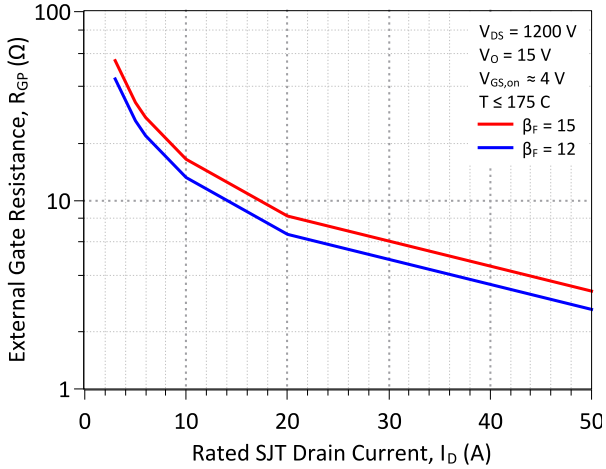

Figure 5 – Suggested R_{GP} values for 1200 V, GAXXJTXX series SJTs for V_O = 15 V.

presence of the parallel resistor and capacitor on the gate driver IC output produces a dynamic gate current waveform due to the presence of a transient gate current peak from the charging of C_{GP} which turns the SJT on and off more quickly and also reduces device losses. An example of this can be seen in the Fig. 4 gate current waveform. Adjusting the gate resistor R_{GP}, capacitor C_{GP}, and gate driver output voltage V_O will alter the static and dynamic performance of the SJT with a tradeoff of switching speed to device and driver losses to fit the particular applications demands.

Gate Resistance R_{GP}

The gate resistor R_{GP} is an external resistor in parallel with an external gate capacitor C_{GP}. R_{GP} and C_{GP} dictate the gate current entering into the

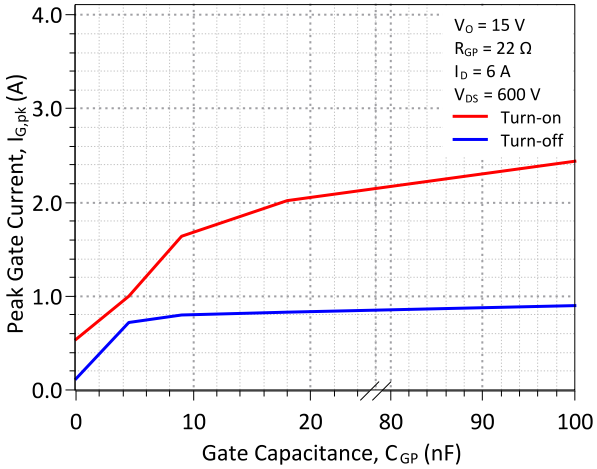

Figure 6 – Effect of external gate capacitance C_{GP} on peak gate current $I_{G,pk}$.

SJT gate during turn-on, forward steady state, and turn-off, as shown in Fig. 4. Of these, the steady state gate current $I_{G,SS}$ during forward steady state is determined by R_{GP}. The $I_{G,SS}$ value after turn-on transients are complete is calculated by the equation

$$I_{G,ss} = \frac{V_O - V_{GS,on}}{R_{GP}}, \qquad (1)$$

in which $V_{GS,on} \approx 4$ V. R_{GP} must be chosen in tandem with V_O to satisfy the I_G drive requirements as shown on the SJT device datasheet for the desired drain current I_D. For optimal SJT performance in many applications, it is suggest to overdrive the SJT by supplying more gate current than absolutely necessary to ensure operation across all rated temperatures with a low V_{DS} value. This can be considered as having a lower effect current gain or "forced" current gain β_F in the range of approximately $12 < \beta_F < 15$ for GAXXJTXX series SJTs. R_{GP} and I_G should be as low as practical given this consideration and approximate R_{GP} values for a range of 1200 V SJT current rating is shown in Fig. 5. R_{GP} = 22 Ω has shown good results for V_{GG} = 15 V.

Gate Capacitance C_{GP}

The presence of C_{GP} produces a transient gate current peak which speeds up the charging of the internal SJT gate capacitance and increases SJT switching speeds. For a fixed driver output voltage V_O, higher capacitance will cause larger current peaks as shown in Fig. 6 where C_{GP} values from 0

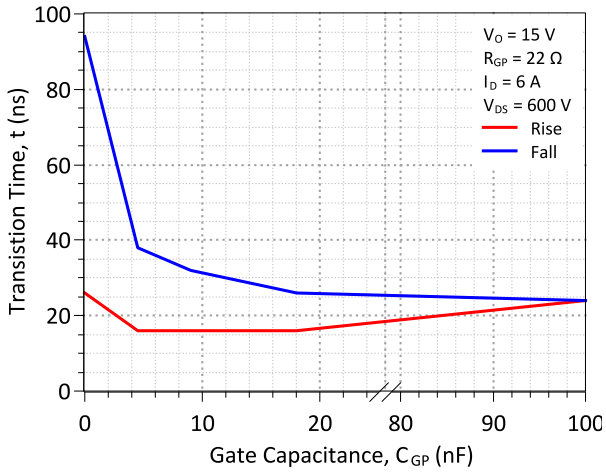

Figure 7 – Effect of external gate capacitance C_{GP} on device turn-on t_r and turn-off t_f times.

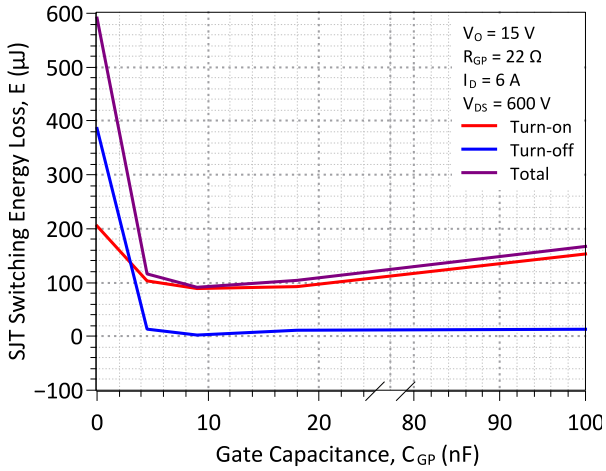

Figure 8 – Effect of gate capacitance C_{GP} on device energy losses.

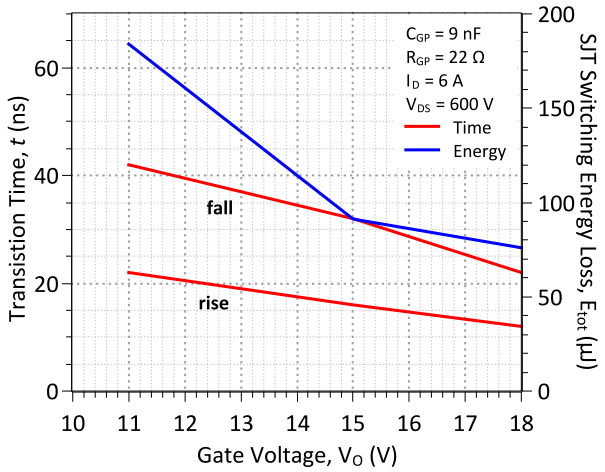

Figure 9 – Effect of gate capacitance C_{GP} on device energy losses.

TABLE II – OPTIMAL DRIVE PARAMETERS FOR 1200 V/6 A SJT

Parameter	Suggested Value
V_O, V_{GG}	15 V
R_{GP}	22 Ω
C_{GP}	9 nF

nF (only R_{GP} present) to 100 nF are compared. Higher gate current peaks correlate with faster I_D rise and fall times in the SJT, particularly fall times, as shown in Fig. 7, however the speeds saturate or decrease for C_{GP} > 18 nF.

The value of C_{GP} also affects device losses E_{on} and E_{off}. This is shown in Fig. 8, in which SJT device losses are lowest for C_{GP} = 9 nF. Any increase or decrease in capacitance value causes a sudden or subtle change in device loss.

Excessive capacitance also increases driver losses due to the power required to charge C_{GP} as shown by the equation

$$P_{\text{drive,sw}} = f_S \, C_{GP}(V_O - V_{GS})^2. \qquad (2)$$

Therefore, C_{GP} should be set to be as low as practical to minimize both device and driver losses while still obtaining desired switching speeds. Ringing may occur in the gate drive output network due to C_{GP}, and the parasitic inductances in the gate drive circuit. To reduce this, a low inductance resistor of 1Ω may be placed in series with C_{GP} to damp this oscillation. C_{GP} = 9 nF is a suggested value in most applications.

Gate Driver Voltage V_O

The gate driver output voltage V_O also affects SJT performance and is adjustable. V_O must be sufficiently high to bias the SJT gate-source junction on, which has a built-in voltage of ~ 2.8 V, and also to supply the steady state gate current $I_{G,SS}$, after the gate current peak, according to equation (1). In Fig. 9, it is shown that there is a nearly linear decrease in E_{tot}, t_r, and t_f with increasing V_O for fixed C_{GP} and R_{GP} values. Thus there is no tradeoff of device switching performance for higher V_O, unlike C_{GP}. However, V_O is known to be a large contributor to gate driver loss in Equation 2 as well as steady state driver losses (detail in document AN-10B), thus there are drawbacks to excessive V_O. Circuit designers should balance their requirements for device switching speed with driver power losses. V_O = 15 V is an appropriate value for 1200 V SJTs in most applications.

TABLE III – GATE DRIVE POWER LOSS EXAMPLE

D = 0.7, f_0 = 500 kHz	
Parameter	**Power Loss**
$P_{drive,ss}$	3.85 W
$P_{drive,sw}$	0.54 W
$P_{SJT,sw}$	45.6 W
Total	**50.0 W**

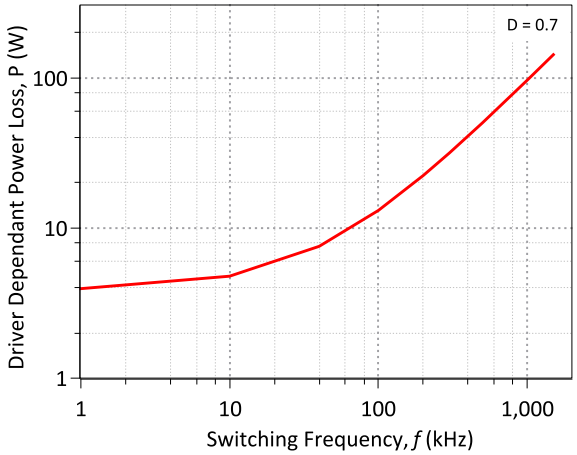

Figure 10 – Gate driver dependent system power loss as a function of frequency for a fixed duty cycle of D = 0.7. Note that the SJT conduction loss component is not considered here.

Power Loss

When the single-level gate driver is utilized with optimal drive parameters to drive a 1200 V / 6 A SJT, the system power losses components in both the gate drive and SJT which are dependent on the gate driver topology are provided in Table III. In this example case the switching frequency is f = 500 kHz and D = 0.7, which is within the capabilities of the SJT and the driver. The steady state losses of the driver $P_{drive,SS}$ are primarily duty cycle dependant while the switching losses of both ($P_{drive,sw}$ and $P_{SJT,sw}$) are frequency and driver dependant. $P_{SJT,sw}$ begins to dominate the system power loss for f > ~ 70 kHz as shown in Fig. 10, where system losses increase linearly with higher switching frequency.

Summary

SJTs are high-performance SiC switches capable of fast switching speeds with ultra-low losses without the drawbacks of other SiC transistors or bipolar Si devices. A simple gate drive schematic has been presented along with resultant device switching performance. More detailed considerations of passive component value selection is also discussed with benefits and drawbacks explained. More advanced SJT gate drive schematics are discussed in document AN-10B and future GeneSiC Semiconductor application notes.

References

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