

# G3R20MT17K

## 1700 V 20 mΩ SiC MOSFET



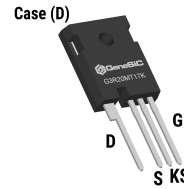
Silicon Carbide MOSFET  
N-Channel Enhancement Mode

$V_{DS}$	=	1700 V
$R_{DS(ON)(Typ.)}$	=	20 mΩ
$I_D(T_C = 100^\circ\text{C})$	=	67 A

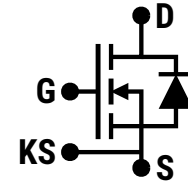
### Features

- G3R™ Technology with +15 V Gate Drive
- Softer  $R_{DS(ON)}$  v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller  $R_{G(INT)}$  and Lower  $Q_G$
- Low Device Capacitances ( $C_{OSS}$ ,  $C_{RSS}$ )
- Superior Cost-Performance Index
- Robust Body Diode with Low  $V_F$  and Low  $Q_{RR}$
- Industry-Leading UIL & Short-Circuit Robustness

### Package



TO-247-4



D = Drain  
G = Gate  
S = Source  
KS = Kelvin Source



### Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Better Power Density and System Efficiency
- Ease of Paralleling without Thermal Runaway
- Superior Robustness and System Reliability

### Applications

- EV Fast Charging
- Solar Inverters
- Industrial Motor Drives
- Transportation
- Industrial Power Supply
- Smart Grid and HVDC
- Induction Heating and Welding
- Pulsed Power

### Absolute Maximum Ratings (At $T_C = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	$V_{GS} = 0\text{ V}$ , $I_D = 100\ \mu\text{A}$	1700	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +20	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +15	V	
Continuous Forward Current	$I_D$	$T_C = 25^\circ\text{C}$ , $V_{GS} = -5 / +15\text{ V}$	95	A	Fig. 15
		$T_C = 100^\circ\text{C}$ , $V_{GS} = -5 / +15\text{ V}$	67		
		$T_C = 135^\circ\text{C}$ , $V_{GS} = -5 / +15\text{ V}$	49		
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq 3\ \mu\text{s}$ , $D \leq 1\%$ , $V_{GS} = 15\text{ V}$ , Note 1	250	A	Fig. 14
Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	569	W	Fig. 16
Non-Repetitive Avalanche Energy	$E_{AS}$	$L = 2.0\text{ mH}$ , $I_{AS} = 37.5\text{ A}$	1410	mJ	
Operating and Storage Temperature	$T_j$ , $T_{stg}$		-55 to 175	$^\circ\text{C}$	

### Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Case	$R_{thJC}$		0.20	0.26		$^\circ\text{C}/\text{W}$	Fig. 13
Weight	$W_T$		6.2			g	
Mounting Torque	$T_M$	Screws to Heatsink			1.1	Nm	

Note 1: Pulse Width  $t_P$  Limited by  $T_{j(max)}$

**Electrical Characteristics (At  $T_C = 25^\circ\text{C}$  Unless Otherwise Stated)**

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{DSS}$	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	1700			V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 1700\text{ V}, V_{GS} = 0\text{ V}$		1		$\mu\text{A}$	
Gate Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$			-100		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 60.0\text{ mA}$	1.8	2.70		V	Fig. 9
		$V_{DS} = V_{GS}, I_D = 60.0\text{ mA}, T_j = 175^\circ\text{C}$		1.90			
Transconductance	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 75\text{ A}$		37.9		S	Fig. 4
		$V_{DS} = 10\text{ V}, I_D = 75\text{ A}, T_j = 175^\circ\text{C}$		39.0			
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 75\text{ A}$		20	28	mΩ	Fig. 5-8
		$V_{GS} = 15\text{ V}, I_D = 75\text{ A}, T_j = 175^\circ\text{C}$		45			
Input Capacitance	$C_{iss}$			7620			
Output Capacitance	$C_{oss}$			205		pF	Fig. 11
Reverse Transfer Capacitance	$C_{rss}$			36.4			
$C_{oss}$ Stored Energy	$E_{oss}$	$V_{DS} = 1000\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		136		$\mu\text{J}$	Fig. 12
$C_{oss}$ Stored Charge	$Q_{oss}$			410		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			272		pF	Note 2
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			410			
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 1000\text{ V}, V_{GS} = -5 / +15\text{ V}$		77		nC	Fig. 10
Gate-Drain Charge	$Q_{gd}$	$I_D = 75\text{ A}$		90			
Total Gate Charge	$Q_g$	Per IEC607478-4		256			
Internal Gate Resistance	$R_{G(int)}$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		1.8		$\Omega$	
Turn-On Switching Energy (Body Diode)	$E_{on}$	$T_j = 25^\circ\text{C}, V_{GS} = -5/+15\text{ V}, R_{G(ext)} = 0.5\ \Omega, L = 32.0\ \mu\text{H}, I_D = 75\text{ A}, V_{DD} = 1200\text{ V}$		892		$\mu\text{J}$	Fig. 22,26
Turn-Off Switching Energy (Body Diode)	$E_{off}$			490			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 1200\text{ V}, V_{GS} = -5/+15\text{ V}$ $R_{G(ext)} = 0.5\ \Omega, L = 32.0\ \mu\text{H}, I_D = 75\text{ A}$ Timing relative to $V_{DS}$ , Inductive load		52		ns	Fig. 24
Rise Time	$t_r$			32			
Turn-Off Delay Time	$t_{d(off)}$			38			
Fall Time	$t_f$			24			

\*The chip technology was characterized up to 200 V/ns. The measured  $dV/dt$  was limited by measurement test setup and package.

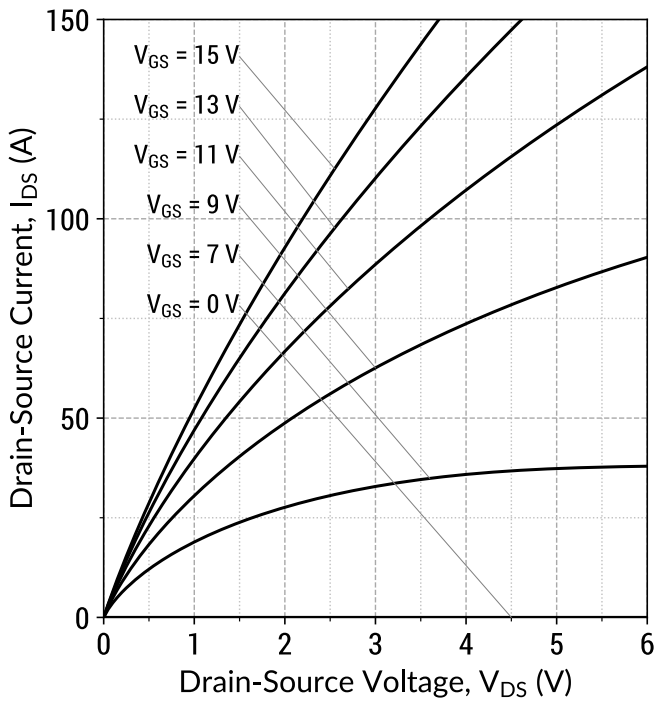
Note 2:  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 1000V.

$C_{o(tr)}$ , a lumped capacitance that gives same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 1000V.

### Reverse Diode Characteristics

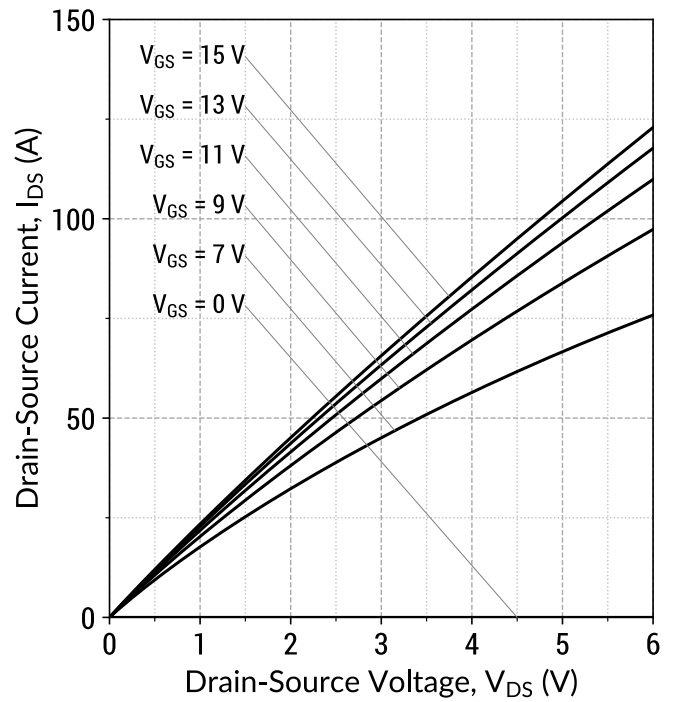
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 37\text{ A}$ $V_{GS} = -5\text{ V}, I_{SD} = 37\text{ A}, T_j = 175^\circ\text{C}$		4.4 4.2		V	Fig. 17-18
Continuous Diode Forward Current	$I_S$	$V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$	58			A	
Diode Pulse Current	$I_{S(pulse)}$	$V_{GS} = -5\text{ V}, \text{Note 1}$		232		A	
Reverse Recovery Time	$t_{rr}$			63		ns	
Reverse Recovery Charge	$Q_{rr}$	$V_{GS} = -5\text{ V}, I_{SD} = 75\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 800\text{ A}/\mu\text{s}, T_j = 25^\circ\text{C}$		752		nC	
Peak Reverse Recovery Current	$I_{rrm}$			21		A	
Reverse Recovery Time	$t_{rr}$			108		ns	
Reverse Recovery Charge	$Q_{rr}$	$V_{GS} = -5\text{ V}, I_{SD} = 75\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 800\text{ A}/\mu\text{s}, T_j = 175^\circ\text{C}$		2820		nC	
Peak Reverse Recovery Current	$I_{rrm}$			45		A	

Figure 1: Output Characteristics ( $T_j = 25^\circ\text{C}$ )



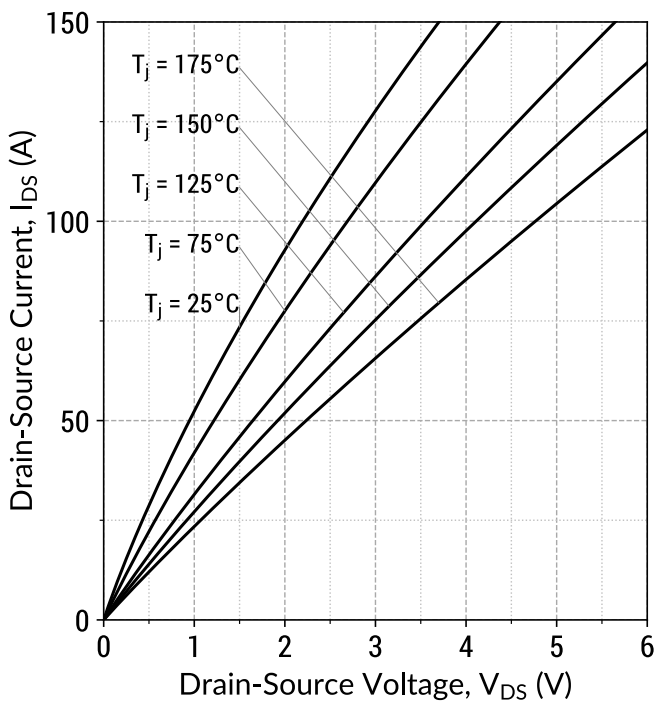
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 2: Output Characteristics ( $T_j = 175^\circ\text{C}$ )



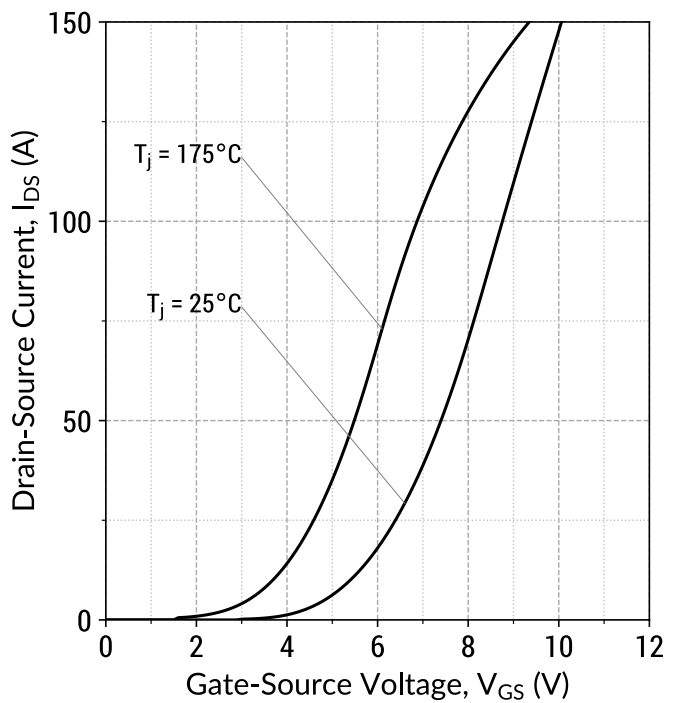
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 3: Output Characteristics ( $V_{GS} = 15\text{ V}$ )



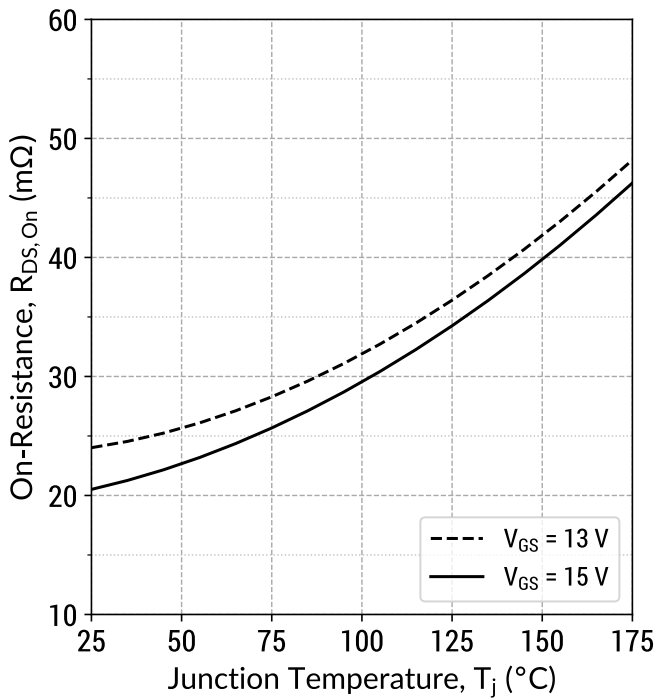
$I_D = f(V_{DS}, T_j); t_P = 250 \mu\text{s}$

Figure 4: Transfer Characteristics ( $V_{DS} = 10\text{ V}$ )



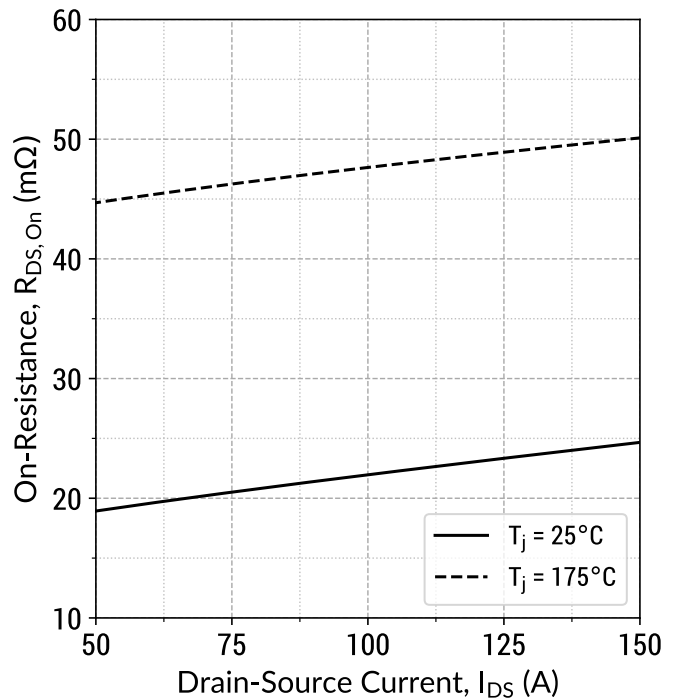
$I_D = f(V_{GS}, T_j); t_P = 100 \mu\text{s}$

Figure 5: On-State Resistance v/s Temperature



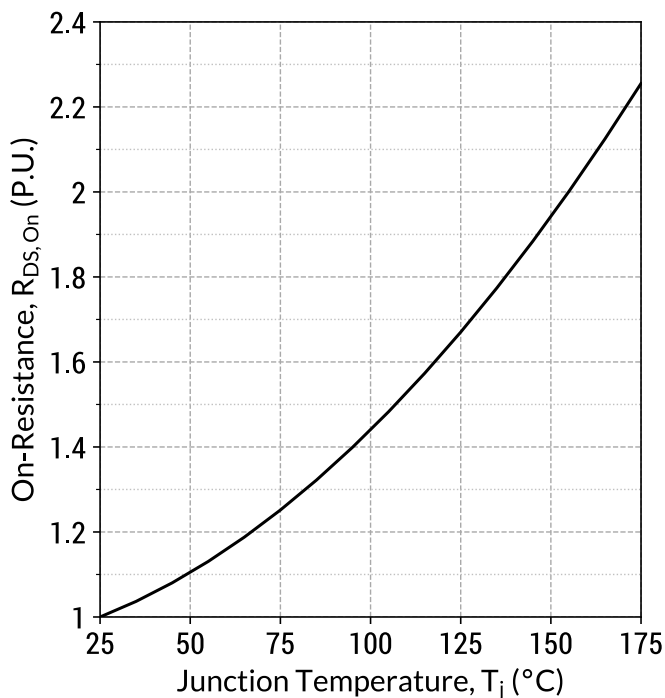
$R_{DS(on)} = f(T_j, V_{GS}); t_P = 250\ \mu\text{s}; I_D = 75\text{ A}$

Figure 6: On-State Resistance v/s Drain Current



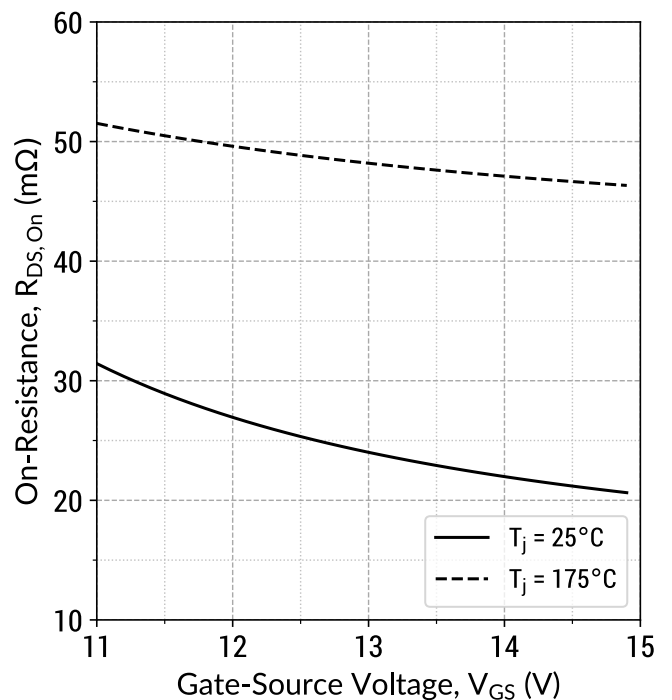
$R_{DS(on)} = f(T_j, I_D); t_P = 250\ \mu\text{s}; V_{GS} = 15\text{ V}$

Figure 7: Normalized On-State Resistance v/s Temperature



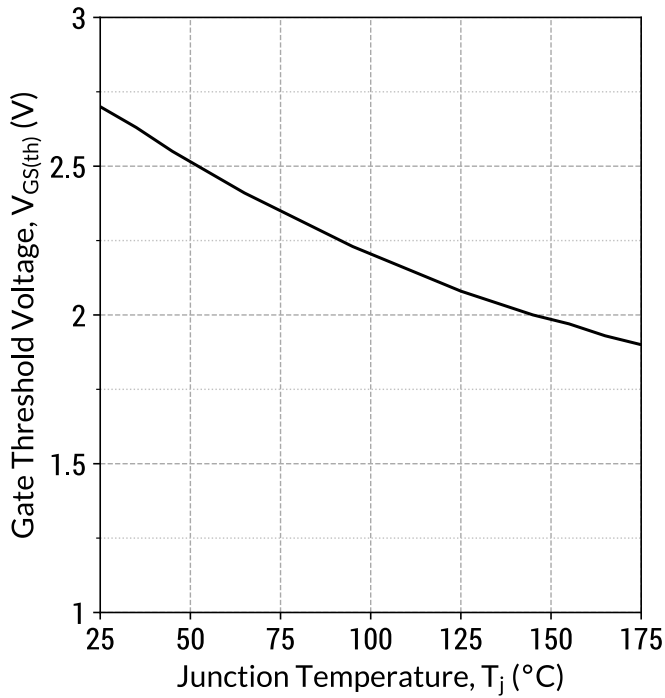
$R_{DS(on)} = f(T_j); t_P = 250\ \mu\text{s}; I_D = 75\text{ A}; V_{GS} = 15\text{ V}$

Figure 8: On-State Resistance v/s Gate Voltage



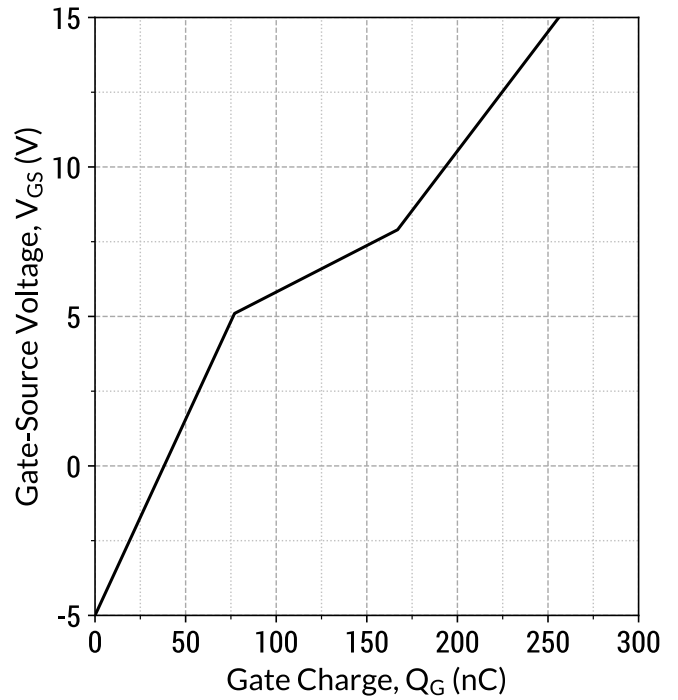
$R_{DS(on)} = f(T_j, V_{GS}); t_P = 250\ \mu\text{s}; I_D = 75\text{ A}$

Figure 9: Threshold Voltage Characteristics



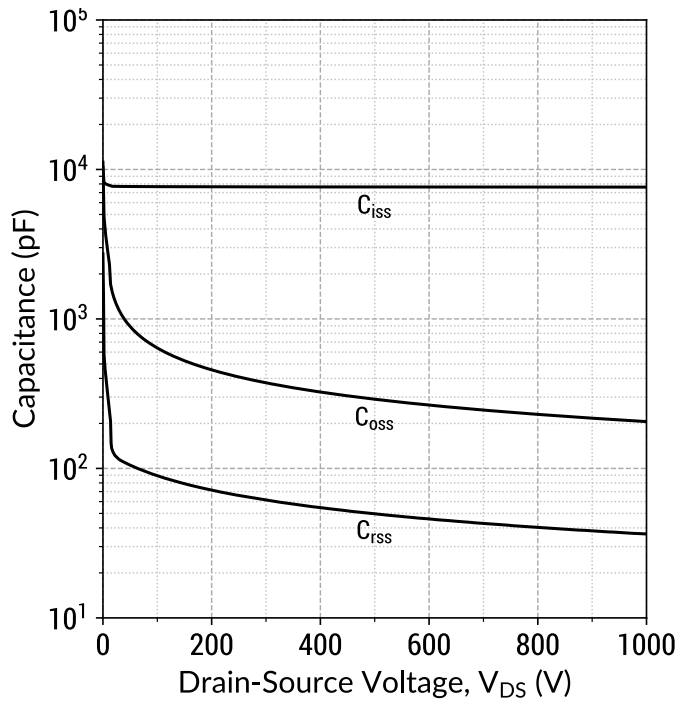
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 60.0 \text{ mA}$

Figure 10: Gate Charge Characteristics



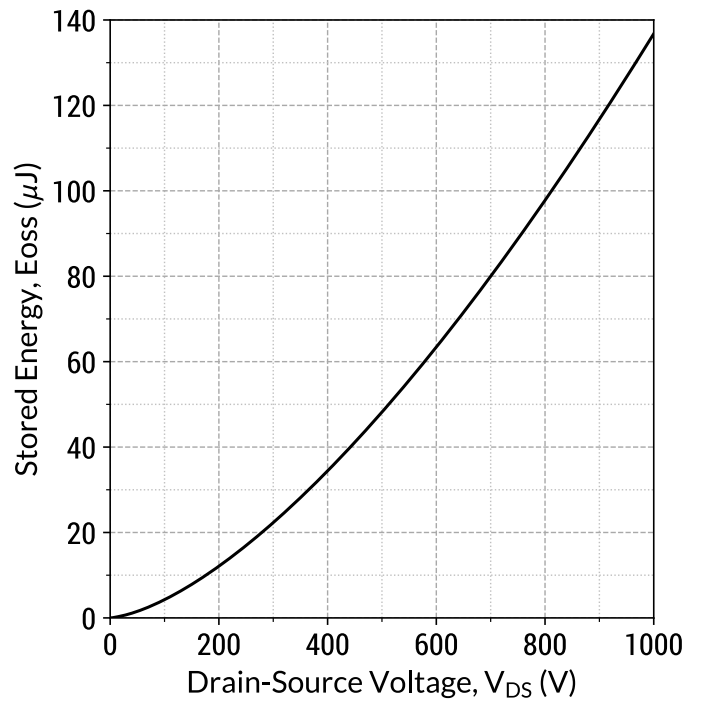
$I_D = 75 \text{ A}; V_{DS} = 1000 \text{ V}; T_C = 25^\circ\text{C}$

Figure 11: Capacitance v/s Drain-Source Voltage



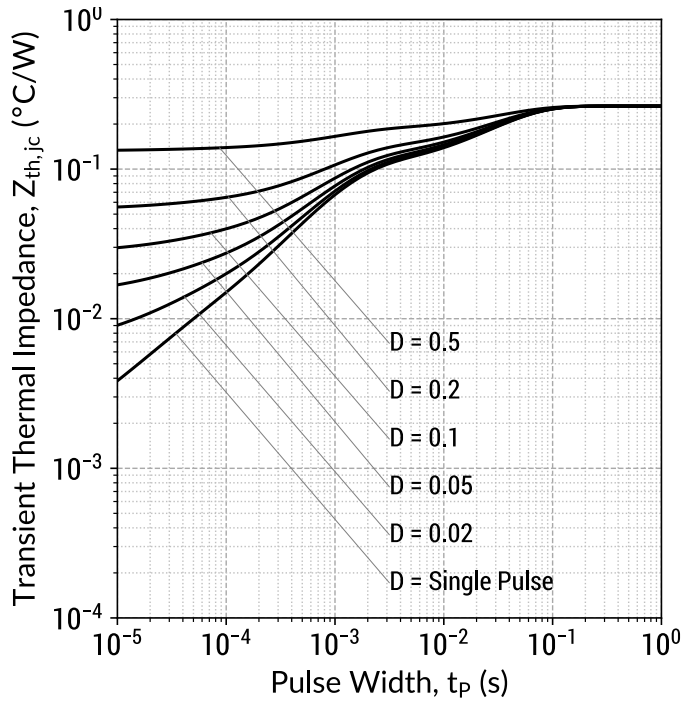
$f = 1 \text{ MHz}; V_{AC} = 25\text{mV}$

Figure 12: Output Capacitor Stored Energy



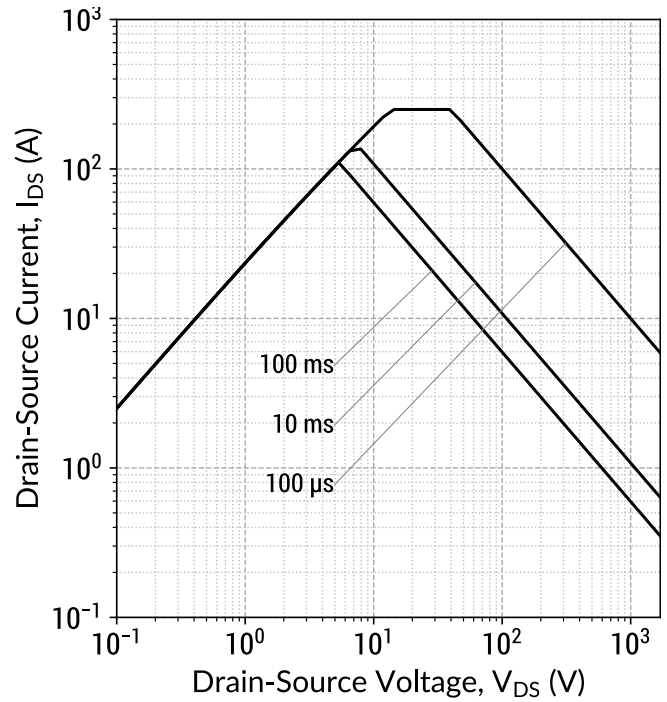
$E_{oss} = f(V_{DS})$

Figure 13: Transient Thermal Impedance



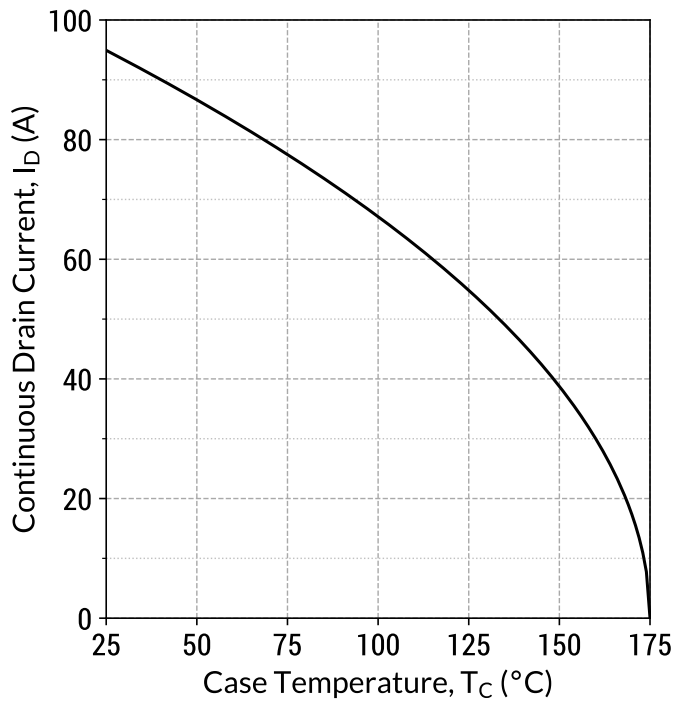
$$Z_{th,jc} = f(t_p, D); D = t_p/T$$

Figure 14: Safe Operating Area ( $T_c = 25^\circ\text{C}$ )



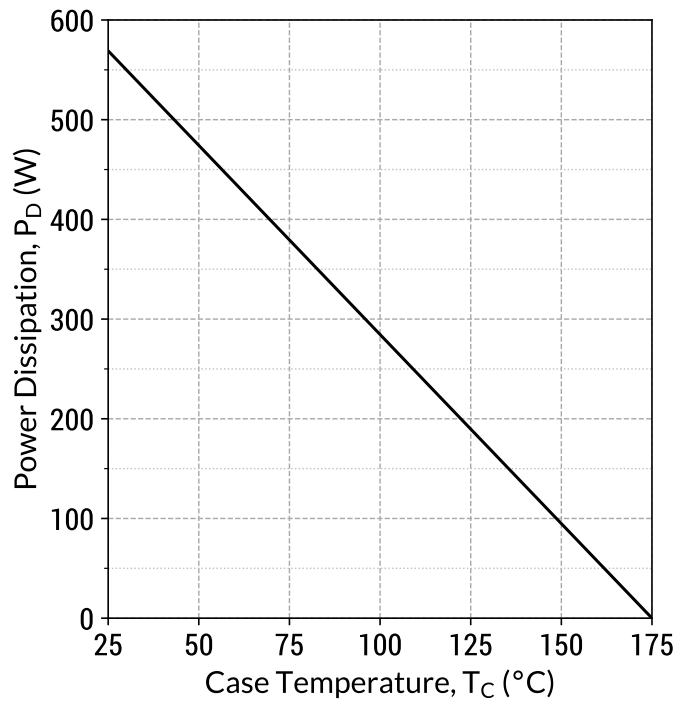
$$I_D = f(V_{DS}, t_p); T_j \leq 175^\circ\text{C}; D = 0$$

Figure 15: Current De-rating Curve



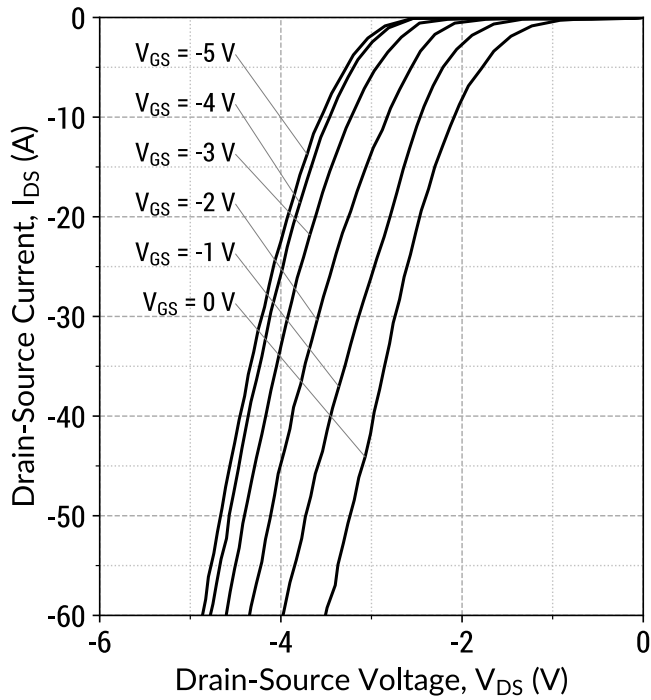
$$I_D = f(T_C); T_j \leq 175^\circ\text{C}$$

Figure 16: Power De-rating Curve



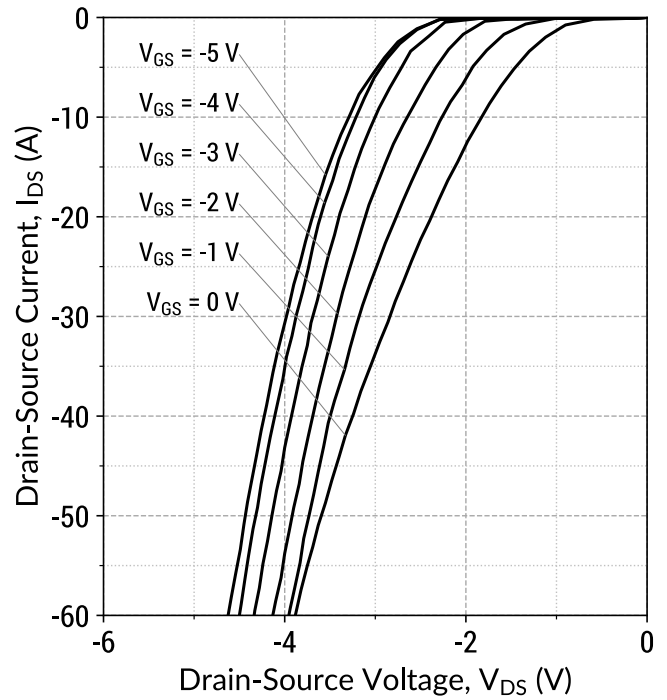
$$P_D = f(T_C); T_j \leq 175^\circ\text{C}$$

Figure 17: Body Diode Characteristics ( $T_j = 25^\circ\text{C}$ )



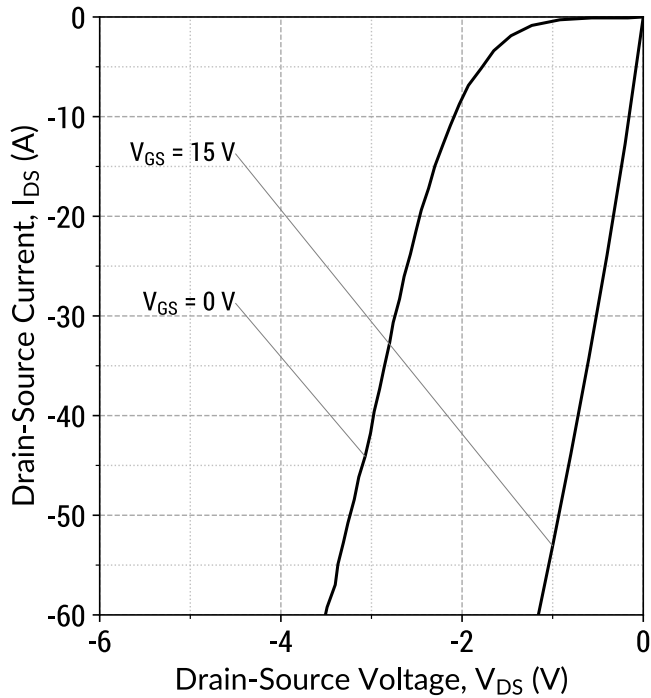
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 18: Body Diode Characteristics ( $T_j = 175^\circ\text{C}$ )



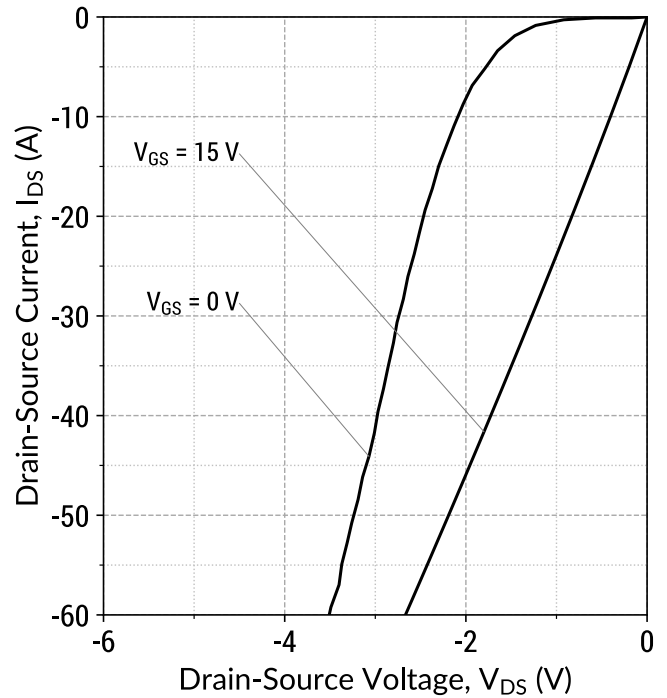
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 19: Third Quadrant Characteristics ( $T_j = 25^\circ\text{C}$ )



$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

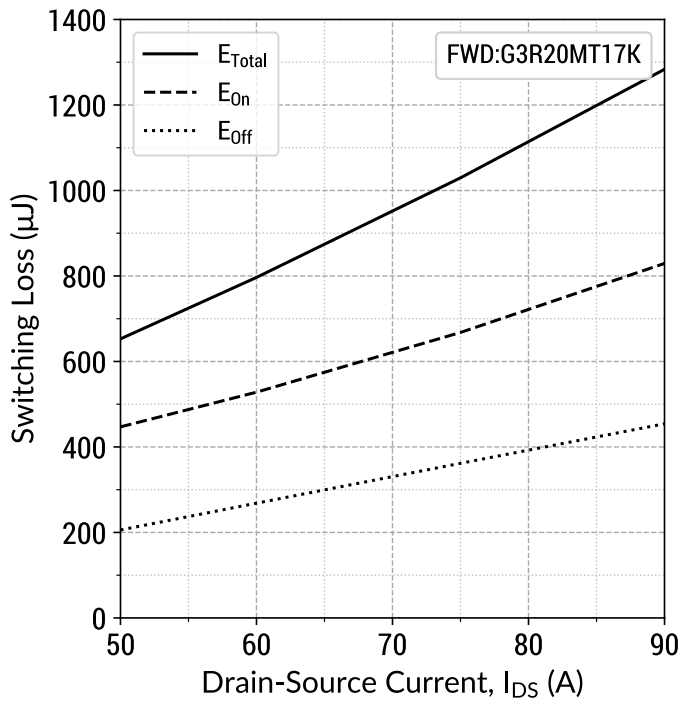
Figure 20: Third Quadrant Characteristics ( $T_j = 175^\circ\text{C}$ )



$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

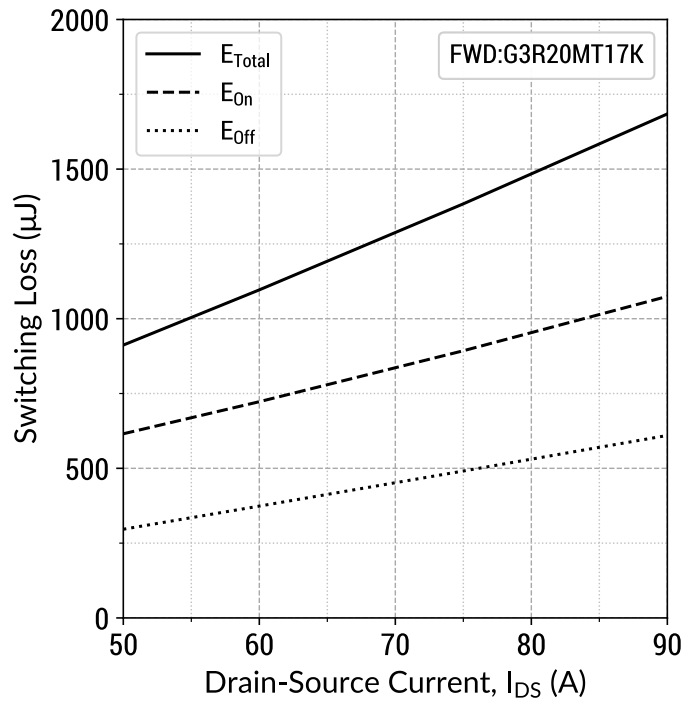


Figure 21: Inductive Switching Energy v/s Drain Current ( $V_{DD} = 1000V$ )



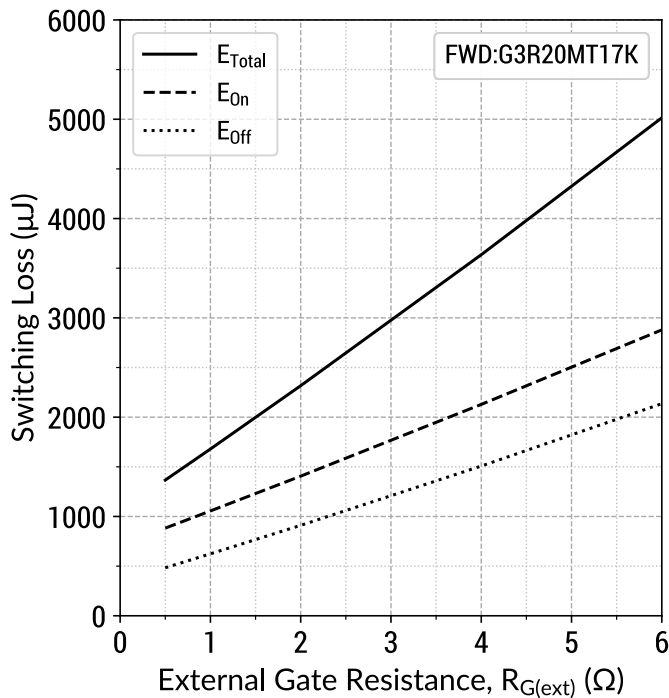
$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $R_{G(ext)} = 0.5 \Omega$ ;  $L = 32.0 \mu H$

Figure 22: Inductive Switching Energy v/s Drain Current ( $V_{DD} = 1200V$ )



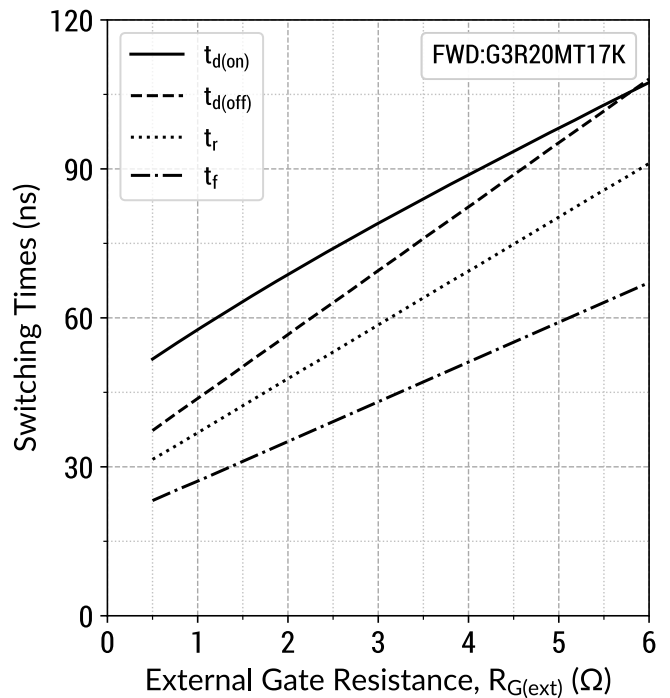
$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $R_{G(ext)} = 0.5 \Omega$ ;  $L = 32.0 \mu H$

Figure 23: Inductive Switching Energy v/s  $R_{G(ext)}$  ( $V_{DD} = 1200V$ )



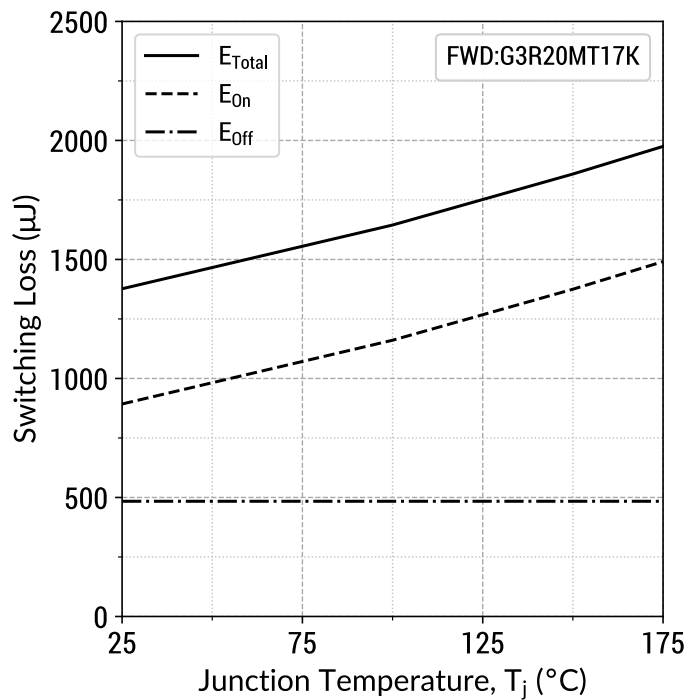
$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $I_{DS} = 75 A$ ;  $L = 32.0 \mu H$

Figure 24: Switching Time v/s  $R_{G(ext)}$  ( $V_{DD} = 1200V$ )



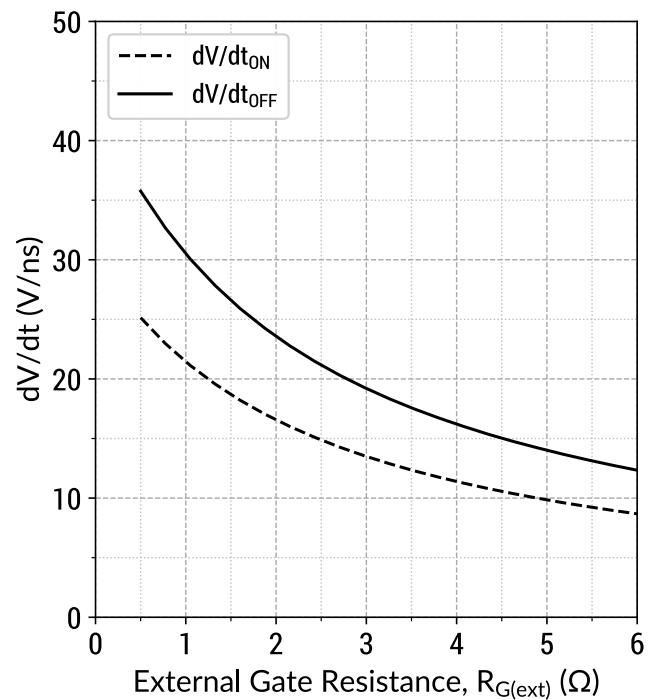
$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $I_{DS} = 75 A$ ;  $L = 32.0 \mu H$

Figure 25: Inductive Switching Energy v/s Temperature  
( $V_{DD} = 1200V$ )



$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $R_{G(ext)} = 0.5 \Omega$ ;  $I_{DS} = 75 A$ ;  $L = 32.0 \mu H$

Figure 26:  $dV/dt$  v/s  $R_{G(ext)}$   
( $V_{DD} = 1200V$ )

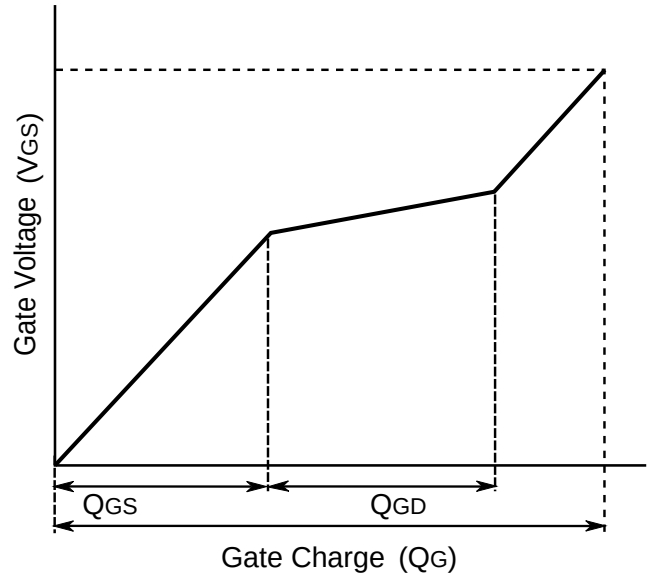


$T_j = 25^\circ C$ ;  $V_{GS} = -5/+15V$ ;  $I_{DS} = 75 A$ ;  $L = 32.0 \mu H$

Gate Charge Circuit



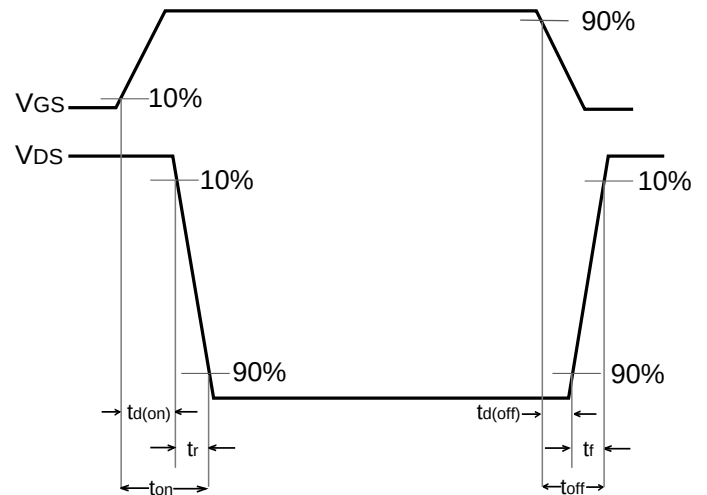
Gate Charge Waveform



Switching Time Circuit



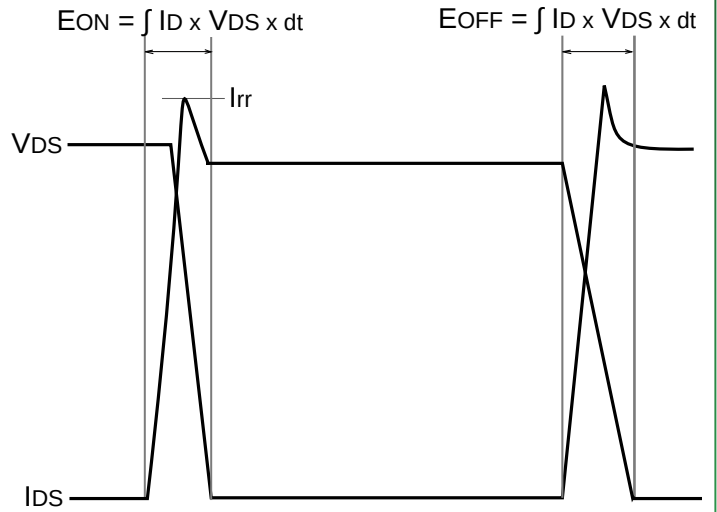
Switching Time Waveform



Switching Energy Circuit



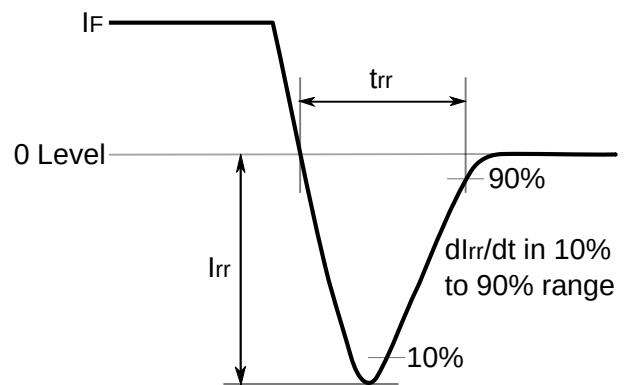
Switching Energy Waveform



Reverse Recovery Circuit

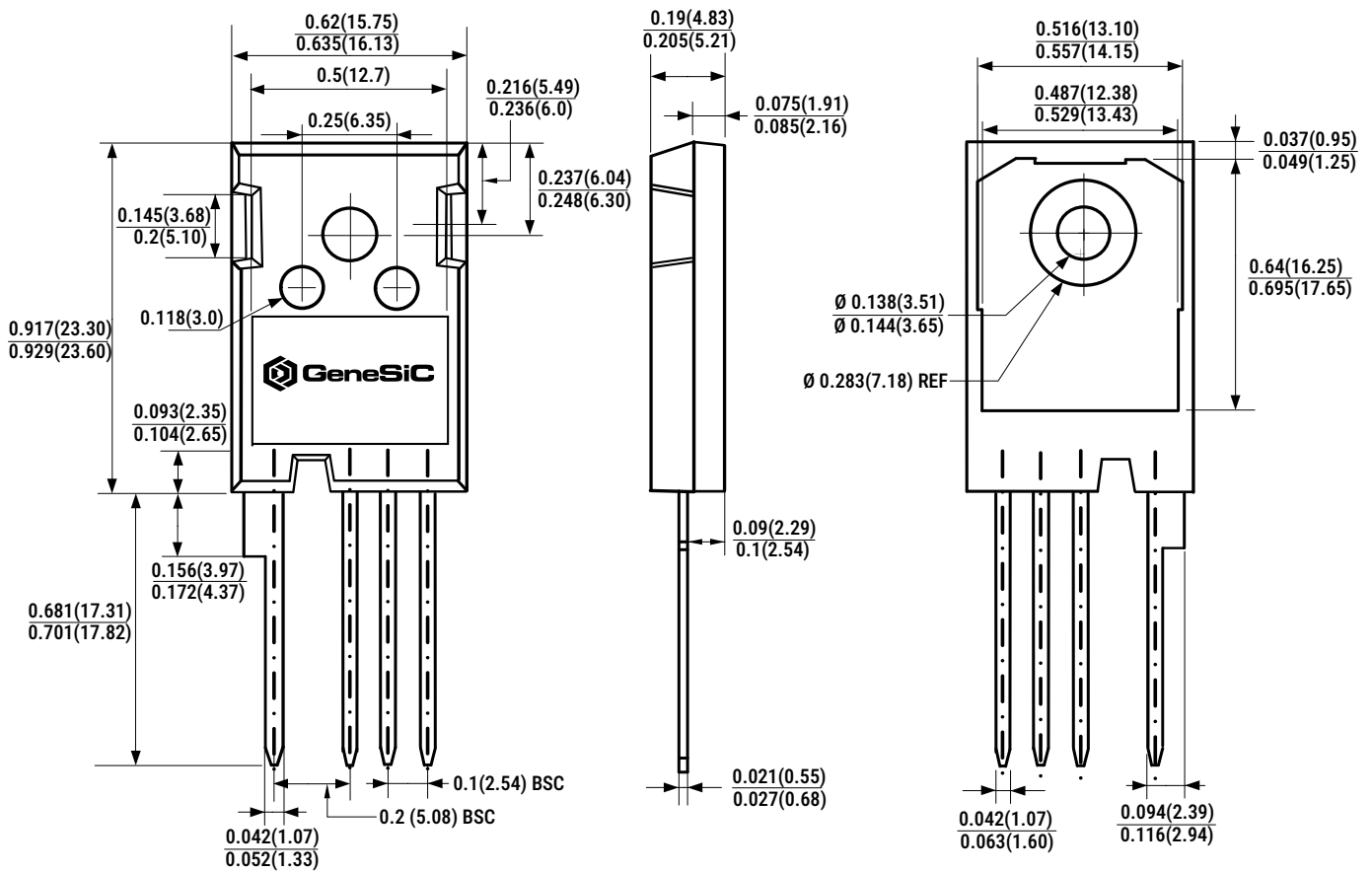


Reverse Recovery Waveform

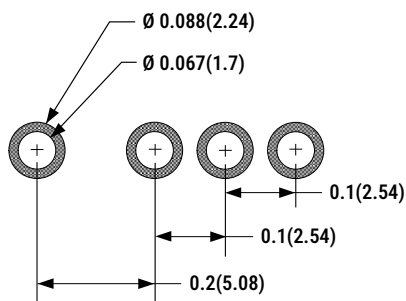


Package Dimensions

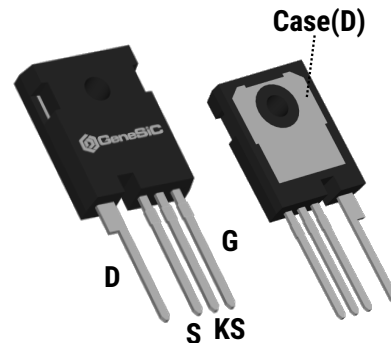
TO-247-4 Package Outline



Recommended Solder Pad Layout



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

## Compliance

### RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

### REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

## Disclaimer

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Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

## Related Links

- SPICE Models: [https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K\\_SPICE.zip](https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_SPICE.zip)
- PLECS Models: [https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K\\_PLECS.zip](https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_PLECS.zip)
- CAD Models: [https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K\\_3D.zip](https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_3D.zip)
- Gate Driver Reference: <https://www.genesicsemi.com/technical-support>
- Evaluation Boards: <https://www.genesicsemi.com/technical-support>
- Reliability: <https://www.genesicsemi.com/reliability>
- Compliance: <https://www.genesicsemi.com/compliance>
- Quality Manual: <https://www.genesicsemi.com/quality>

## Revision History

- Rev 21/May: Updated switching time and switching energy data
- Supersedes: Rev 20/Jun, Rev 20/Sep, Rev 21/Feb



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