GeneSiC Semiconductor Reliability Report on

1200 V SiC Schottky Rectifiers

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1. Report Summary

This report summarizes the reliability qualification of GeneSiC Semiconductor 1200 V SiC Schottky rectifiers. Theses device come in numerous current ratings and package types. The report includes complete, on-going and planned reliability testing procedures and results. The reliability standards herein are based on industry standard reference documents the Automotive Electronics Council's (AEC) *Stress Test Qualification for Automotive Grade Discrete Semiconductors* (AEC-Q101, Rev. D) and JEDEC's *Stress-Test-Driven Qualification of Integrated Circuits* (JESD47-I). These two documents reference numerous other reliability testing standards published by the JEDEC, AEC and MIL-STD.

2. Reliability Test Plan

Table 1 – Reliability test plan summary for 1200 V SiC Schottky rectifiers for full AEC-Q101 Qualification.

Test Name	Test Standard	Test Conditions	Test Duration	DUTs
Pre-Conditioning (PC)	JESD22 A-113	Prior to select SMD device tests		All SMD Devices
External Visual (EV)	JESD22 B-101	Inspect device construction, markings, and workmanship		All Devices
Parametric Verification (PV)		Test all parameters over entire device temperature range		3 Lot X 25 Devices
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038	V_R = 960 V, T_{amb} = 175 °C	1000 hr	3 Lot X 77 Devices
Temperature Cycling (TC)	JESD22 A-104, App 6	T_{amb} ramped from -55 °C to 175 °C, 5 min dwell	400 Cycles	3 Lot X 77 Devices
Unbiased Highly Accelerated Stress Test (UHAST)	JESD22 A-118	T_{amb} = 130 °C, 85 % Relative Humidity	96 hr	3 Lot X 77 Devices
High Humidity and High Temperature Bias (H3TRB)	JESD22 A-101	V_R = 100 V, T_{amb} = 85 °C, 85 % Relative Humidity	1000 hr	3 Lot X 77 Devices
Intermittent Operating Life (IOL)	MIL-STD-750-1 M1037	15 000 Cycles, I_D = 3 A for 60 s until ΔT_j = 100 °C, then remove bias for 180 s until T_j = 25 °C*	1000 hr	3 Lot X 77 Devices
Wire Bond Integrity (WBI)	MIL-STD-750-2 M2037	T_{amb} = 175 °C, Decapsulate and wire pull inspect all wire bonds	500 hr	3 Lot X 5 Devices
ESD Human Body Model (HBM)	AEC-Q101-001			1 Lot X 30 Devices
ESD Charged Device Model (CDM)	AEC-Q101-005			1 Lot X 30 Devices
Destructive Physical Analysis (DPA)	AEC-Q101-004, Sec. 4	50 X Magnification inspection for physical defects		3 Lot X 2 Devices (TC and H3TRB Device)

*** Conditions given for 1200 V / 2 A Schottky rectifier, bias conditions will vary by device current rating and package thermal characteristics.**

3. Reliability Test Descriptions

Pre-Conditioning (PC) - SMD parts qualification parts prior to TC, H3TRB & IOL Testing.

External Visual (EV) – Visible inspection of device construction and workmanship to ensure that it is in working order prior to testing.

Parametric Verification (PV) – Testing of tracked device parameters ($V_{DS(BD)}$, I_{DSS}, I_{SG}, $V_{DS(on)}$, and β) over rated temperature range prior to testing to ensure statistical compliance of devices within rated datasheet parameters.

High Temperature Reverse Bias (HTRB) – Test of the blocking reliability of semiconductor device while enduring the device's maximum rated temperature to ensure there is no decrease in blocking voltage or major increase in reverse bias leakage current.

Temperature Cycling (TC) – Cycling of device ambient temperature primarily to ensure reliable packaging of device that will endure device's rated temperature range without degrading which would decrease the power handling capability of the device.

Unbiased Highly Accelerated Stress Test (UHAST) – Devices subjected to an extreme environment without electrical bias to ensure protection from pressurized heated moisture by its packaging.

High Humidity and High Temperature Bias (H3TRB) – Application of low reverse bias voltage within extreme heated, moist environment to ensure device reliance against electrical short circuit during stress.

Intermittent Operating Life (IOL) – Temperature cycling of devices due to self generated heating power from forward biasing without heat sinking ensuring semiconductor and packaging reliability in response to high temperature forward current conduction.

Wire-Bond Integrity (WBI) – Test of device wire bond reliability after maximum temperature stress to ensure current handling capability and ensure proper packaging of device.

Electro Static Discharge Characterization (ESD) – Test of device properties after subjection of ESD charge to ensure durability of device parameters through ESD events.

4. Device Failure Criteria

Devices have three monitored device parameters (MDP) measured before and after stressing, shown in Table 2. Devices are deemed to have failed if a shift of greater than 20 % occurs from pre-test values of either the forward voltage drop or breakdown voltage MDPs measured prior to and after completion of any of the reliability stress experiments listed in the previous sections. A device shall also be deemed a failure if the reverse-bias leakage current at reverse bias increase by greater than 500 % in dry conditions or greater than 1000 % in humid conditions. Final MDP values for each device tested must also be within the device's datasheet minimum and maximum values, or else is will be a failure. Testing may be intermittently broken as allowed by specific test standards to allow device measurement for completeness of results if desired.

Table 2 – Identification of Monitored Device Parameters (MDP) and measurement conditions.

Monitored Device Parameters		Measurement Condition	Failure Criteria
Breakdown Voltage	V_{BD}	I_{DSS} = 1mA	> ± 20 % Change
Leakage Current	I_{RSS}	V_R = 1200 V	> 500 % Increase
Forward Voltage Drop	V_F	I_F = Rated Current	> ± 20 % Change

5. Parameter Verification Data

Parameter verification (PV) data are shown with Monitored Device Parameter (MDP) (V_{BD}, I_{RSS}, V_F) characterization done prior to reliability testing to ensure statistical compliance of devices within rated datasheet parameters (the upper or lower specified limit, LSL or USL). The process capability index (Cpk) of each MDP is also given.

Table 3 – Parameter verification (PV) data of all 1200 V Schottky rectifiers measured at 25 °C.

Parameter	Unit	Spec	Spec	Min	Max	Mean	St. Dev.	C_{pk}
V_{BD}	V	1200	–	1364	1762	1643	78.01	1.892
I_{RSS}	µA	–	10	0.07	8.88	2.84	2.23	1.92
V_F	V	–	2.0	1.38	1.76	1.46	0.06	3.01

6. Reliability Testing Data

The most recently available reliability testing data are presented in this section. All reliability testing is constantly on-going and results will continue to be updated regularly. To date, no devices failures have been observed in any GeneSiC device for any test. Test data currently includes EV, PV, HTRB, TC, UHAST, and IOL results.

Table 4 – Current reliability test data of all 1200 V Schottky rectifiers measured to-date with no failures recorded.

Test Name	Testing Time to Date	Devices Tested	Device Failures
EV	–	All Devices	0
PV	–	All Devices	0
HTRB	127 hr	77	0
TC	305 Cycles	30	0
UHAST	96 hr	30	0
IOL	734 Cycles	77	0

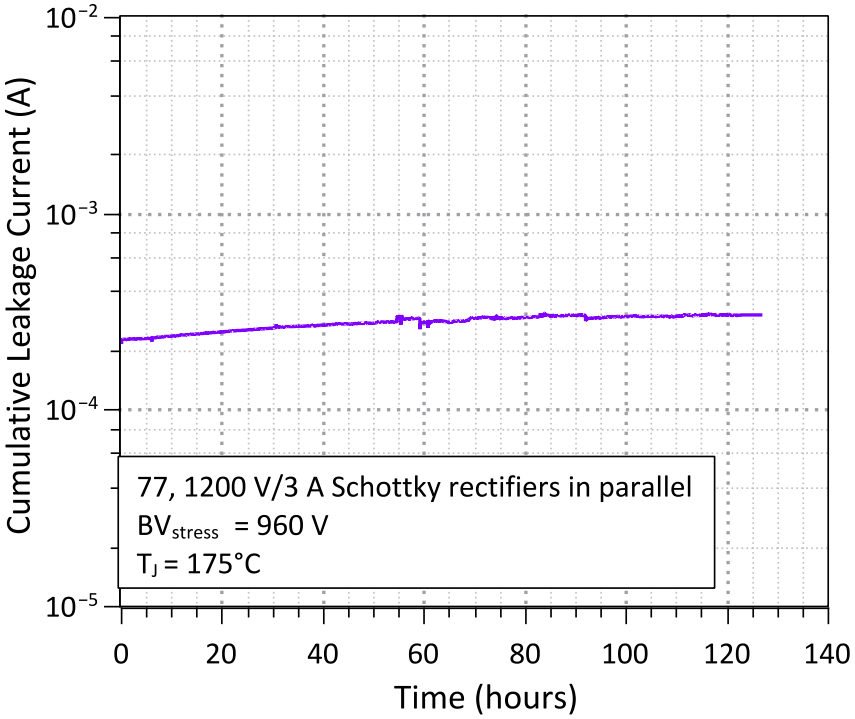

Figure 1 –Reverse bias leakage current IRSS of 77 1200 V SiC Schottky rectifiers in parallel during MIL-STD high-temperature reverse bias (HTRB) testing after 127 test hours. Results show high reliability in response to high-temperature voltage stress. Devices are measured in situ while stressed at BVstress = 960 V, 80 % of the 1200 V rated breakdown voltage as specified in MIL-STD-750-1 M 1038.

7. Conclusion

This report summarizes GeneSiC Semiconductor's comprehensive reliability test plan for 1200 V SiC Schottky rectifiers based on AEC, JEDEC, and MIL-STD standards. A comprehensive list of devices covered by this report can be found on the GeneSiC website*. Reliability testing of these devices is constantly being performed to meet these certifications. Thus far, **zero GeneSiC Semiconductor devices have failed any reliability test to-date** and all devices have thus far met GeneSiC internal reliability requirements. This document will continue to be updated occasionally to show the most current reliability data available.

*** http://www.genesicsemi.com/index.php/sic-products/schottky**