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Static and Switching Characteristics of 1200 V SiC Junction Transistors with On-chip Integrated Schottky Rectifiers

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***Abstract*— A comprehensive evaluation of high-temperature (up to 200°C) on-state, blocking voltage and switching operation of 1200 V-class SiC Junction Transistors (SJTs) with on-chip integrated Schottky rectifiers is presented in this paper. The SJTs feature current gains of 69 and on-resistance of 6.3 mΩ-cm^2 at room-temperature. The integrated free-wheeling Schottky rectifier displays a 0.9 V knee voltage and low on-resistance of 3.3 mΩ-cm^2 at 25°C. Both the SJT and integrated Schottky rectifier show purely majority carrier characteristics with a desirable positive temperature co-efficient of on-state voltage drop. The integrated devices display robust 1200 V blocking voltages with low-leakage currents and a positive temperature co-efficient of breakdown – a clear signature of avalanche multiplication. Sub-50 ns switching waveforms are observed during hard-switching with an inductive load, due to the lower parasitic inherent to the integrated devices. Promising long-term current gain stability is obtained for the latest generation of SiC SJTs.**

I. Introduction

SiC *npn* BJTs with a square reverse biased safe operating area (RBSOA), and temperature independent fast switching capability are developed and commercialized by GeneSiC Semiconductor as SiC Junction Transistors (SJTs). Breakdown voltages > 10 kV, current gain > 130, low specific on-resistance and improved current gain stability were reported on SiC SJTs [1,2]. This paper presents detailed static and switching performance of a novel 1200 V rated, SiC SJT monolithically integrated with an anti-parallel Schottky rectifier. The Schottky diode integrated SJT offers a significant reduction in the parasitic inductance associated with connecting a discrete anti-parallel diode, which should enable higher frequency switching capability with reduced parasitic oscillations.

II. Device Design and Layout

As shown in Figure 1, the SJT and Schottky rectifier share a common n-type drift layer, and a common edge termination. Inter-device isolation between the SJT and Schottky rectifier is achieved by a proprietary ion-implanted p+ guard ring assisted trench concept. The efficiency of the inter-device high-voltage isolation is identified as one of the most important aspects of the device design; therefore a few variations are explored in this study. The epilayer design of the n-p-n epilayer stack is conducted with a targeted 1200 V rating.

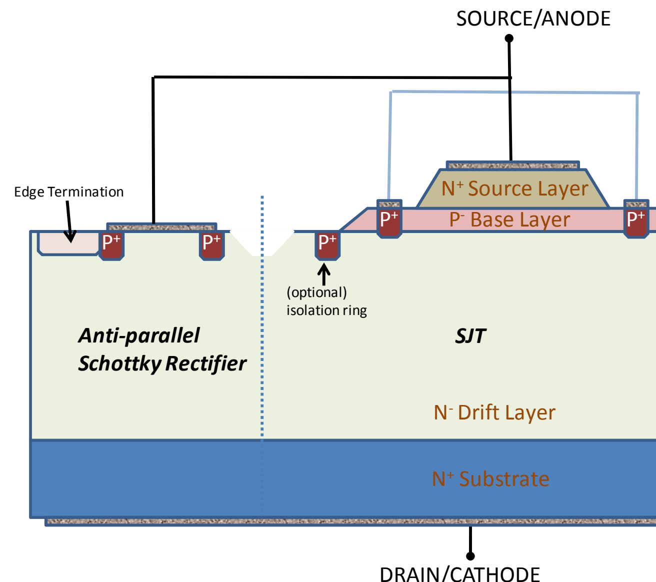

Figure 1. Cross-sectional schematic of the SiC Junctin Transistor integrated with an anti-parallel Schottky rectifier. Note that while this schmeatic shows the SJT in the center of the chip, designs with a centrally located Schottky rectifier are mainly pursued in this study.

Both 650 V and 1200 V rated n-p-n epilayer stacks were used for the device fabrication. Optimized processing recipes

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developed for high-performance SJT fabrication were employed. In addition to the integrated devices, discrete SJTs were also laid out on the same mask set.

The basic device layout for the diode integrated SJT is shown in Figure 2. This design features a centrally located Schottky rectifier with a chip area of 0.94 mm^2. The peripherally located SJT has a 4 mm^2 footprint. The source electrode of the SJT is connected by the overlayer metallization to the anode terminal of the Schottky diode. The SJT and Schottky rectifier share a common edge termination.

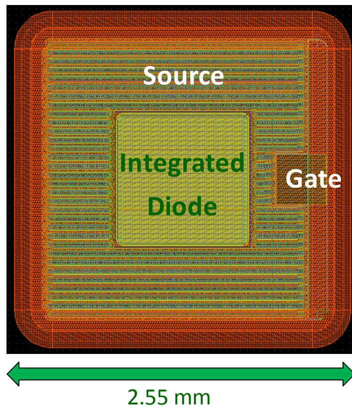

Figure 2. Basic Device Layout of the SiC SJT with the integrated Schottky rectifier.

III. Electrical Characterization

A. On-wafer Breakdown Voltage Characteristics

The on-wafer blocking I-V characteristics measured on 650 V diode-integrated SJTs are shown in Figures 3(a), while the blocking I-V characteristics from 1200 V-rated integrated SJTs are shown in Figure 3(b-c). The breakdown voltages appear to be influenced by the choice of the inter-device isolation design layout. Integrated devices fabricated with design “2” display breakdown voltages comparable to their discrete counterparts. The on-state characteristics of the diode-integrated devices (not shown) are also comparable to the discrete SJTs fabricated on the same SiC wafer.

B. High-Temperature Electrical Characteristics

After comprehensive on-wafer device characterization, selected 1200 V diode-integrated SJTs were diced and packaged in custom TO-257 Au-plated headers, and subjected to high-temperature I-V and switching characterization.

The output characteristics of a packaged 1200 V integrated SJT is shown in Figure 4 at temperatures up to 200°C. In the first quadrant, typical SJT characteristics are observed, with a room temperature current gain of 69, and a low on-resistance of 6.3 mΩ-cm^2, which compare favorably to the discrete SJTs. In the third quadrant, Schottky diode-like I-V characteristics are observed, featuring a room-temperature on-resistance of 3 mΩ-cm^2, and a reasonable knee voltage of 0.9 V. Positive temperature co-efficient of the on-state voltage drop of both the SJT and the integrated diode indicate purely majority carrier operation mode.

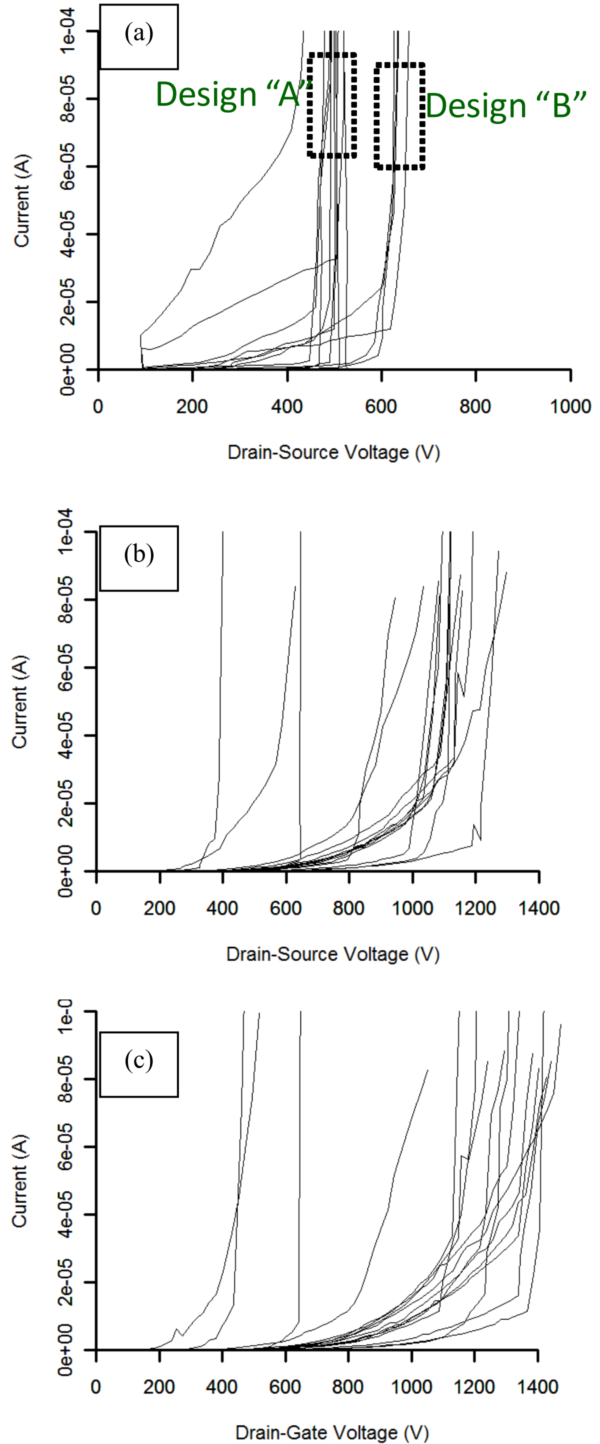

Figure 3. Drain-Source blocking-mode characteristics measured on (a): 650 V diode-integrated SJTs, (b): 1200 V diode-integrated SJTs and (c): Drain-Gate characteristics measured on 1200 V diode-integrated SJTs. Devices fabricated with the inter-device isolation design “B” display superior blocking performance.

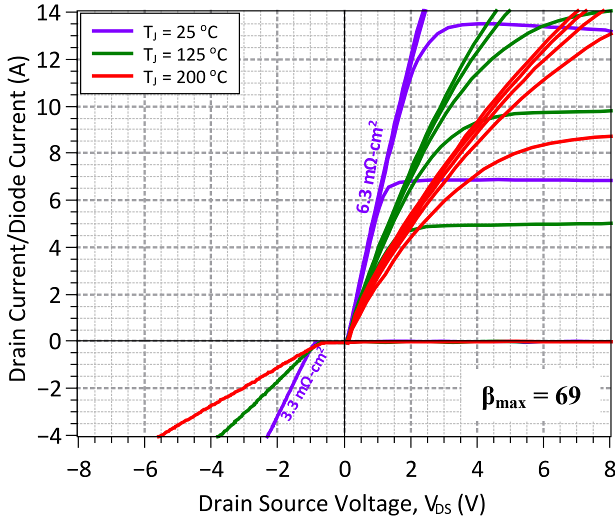

Figure 4. Output characteristics of the SiC integrated-diode SJTs fabricated in this work in the first and third quadrants, at temperatures ranging from 25°C to 200°C.

The blocking characteristics of a packaged diode-integrated SiC SJT are shown in Figure 5 up to temperatures as high as 200°C. Low, μA-level leakage currents are measured even at 200°C, with a clear positive temperature co-efficient of breakdown voltage, which is a signature of pure avalanche breakdown. This result further validates the edge termination/inter-device isolation strategies used for fabricating the integrated SJTs.

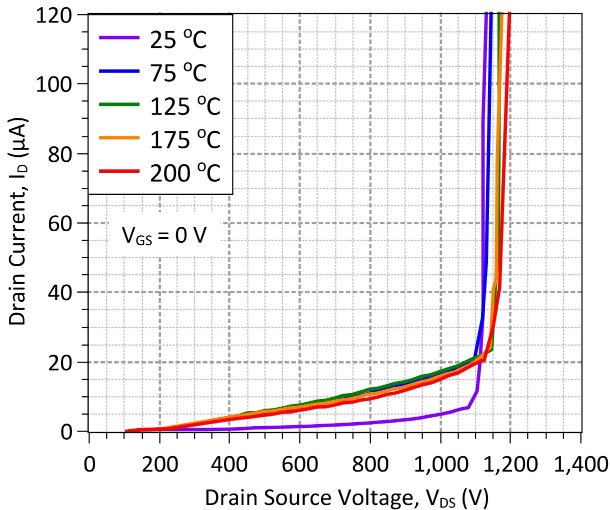

Figure 5. Drain-Source blocking characteristics of a 1200 V SiC integrated-diode SJT measured up to 200°C

C. *Switching Characteristics*

The switching characteristics of the diode integrated SJTs were measured in an inductively loaded circuit configuration, with a standard double pulse scheme to simulate hard switching transients. The switching measurements were performed at a drain voltage of 600 V and a drain current of ≈ 2.5 A by connecting two packaged MIDSJTs in series. The gate and source of the top (inactive) SJT were shorted to prevent it from turning on during the switching measurements. A gate drive scheme previously used to switching discrete SJTs, consisting of a parallel combination of a gate resistor and capacitor was used in this work.

A drain voltage rise time of 40 ns can be inferred from the turn-off switching waveforms shown in Figure 6. The absence of the parasitic inductance inherent to the wire bonds and package capacitance associated with a discrete free-wheeling diode is expected to result in extremely fast switching transients. However, the relatively high parasitic inductances associated with the in-house packaging, and circuit boards currently limit the maximum attainable switching speeds for these devices.

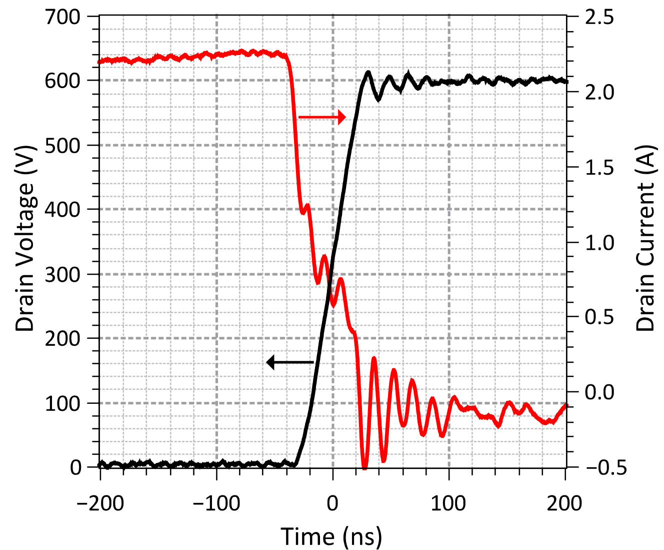

Figure 6. Inductive-load turn-off characteristics of a 1200 V diode-integrated SJT measured at 25°C with a standard double pulse scheme. A standard Si IGBT gate driver was used for the switching measurement.

IV. CURRENT GAIN STABILITY

One of the remaining issues that need to be addressed before widespread commercialization of SiC SJTs is to demonstrate SJT operation with stable current gains over long periods of time, under DC operation, at rated currents, and at high junction temperatures. A comprehensive treatment of this topic can be found in [3]. As compared to the early-stage SJTs focused in [3], significant strides have been made in this area by optimizing key aspects of the materials, device design and process technology. As shown in Figure 7, a 25% reduction in current gain was observed in early stage SJTs, even at modest junction temperatures of 125°C after DC current stressing for 25 hours. By fine-tuning the device and process technology, it has been possible to increase the absolute values of the current gain, in addition to a drastic improvement in current gain stability. SiC SJTs (chip size = 2.25 mm^2) recently fabricated with the Gen-IIIB process display minimal current gain degradation in over 14 hours of testing at a DC drain current stress of 200 A/cm^2 and at a maximum junction temperature as high as 185°C. More detailed testing of the Gen-III SJTs is underway, and the results will be published elsewhere.

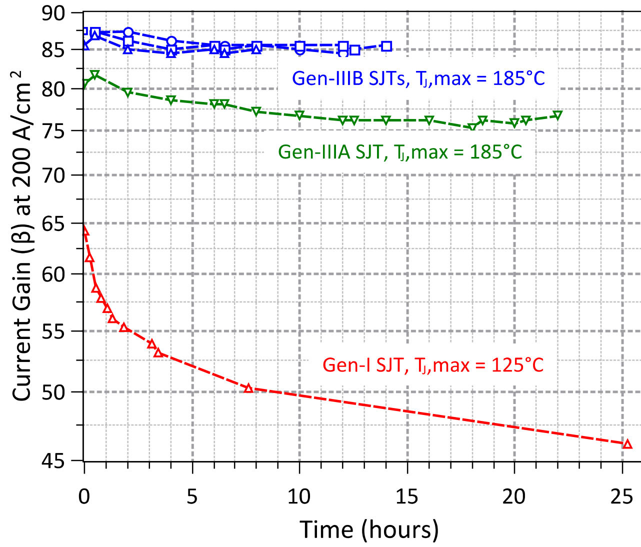

Figure 7. Long-term Current Gain stability of different generations of SiC SJTs , when subjected to DC operation with a drain current of 200 A/cm^2, gate current of 0.5 A, and high junction temperatures.

References

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