Silicon Carbide Junction Transistors and Schottky Rectifiers optimized for 250°C operation

Siddarth Sundaresan, Brian Grummel and Ranbir Singh
GeneSiC Semiconductor, 43670 Trade Center Place, Suite 155, Dulles VA 20166, U.S.A.

ABSTRACT

Electrical performance and reliability of SiC Junction Transistors (SJTs) and Schottky rectifiers are presented. The 650 V/50 A-rated SiC SJTs feature current gains (β) up to 110 at room-temperature, 70 at 250°C, and stable breakdown characteristics. Single current pulse measurements indicate an almost invariant β up to 800 A/cm^2 at 175°C – a measure of the SOA boundary for pulsed current SJT operation. Lower than 5 mA/cm^2 leakage currents are measured on the SJTs at the rated blocking voltage and at 250°C. 1200 V Schottky rectifiers designed for high-temperature operation display < 3 mA/cm^2 leakage currents up to 250°C. A 10x reduction in leakage current and 23% reduction in junction capacitance are observed when compared to the nearest competitor. The high-temperature Schottky rectifiers and SJTs display stable breakdown voltages and on-state characteristics after long-term HTRB stressing. A significant improvement in current gain stability is achieved by fine-tuning the fabrication process.

INTRODUCTION

The 250°C capable SiC Schottky rectifiers and Junction Transistors (SJTs) reported in this paper are targeted at power supply, motor control, and actuator circuits used in oil/gas/downhole and aerospace applications. The poor quality of the SiC MOS interface results in a limited operating range (25°C – 150°C) for the SiC MOSFETs commercialized to-date. Conversely, the absence of a MOS interface in the SiC SJT lends itself to reliable operation at >175°C. The operation of 1200 V SJTs at temperatures as high as 500°C was reported in [1]. This article explores the high-temperature performance and reliability characteristics of 650 V/5 A – 50 A SJTs and 1200 V/0.75 A – 20 A Schottky rectifiers fabricated at GeneSiC. All devices are packaged in JEDEC industry standard through hole (TO-257/258) packages.

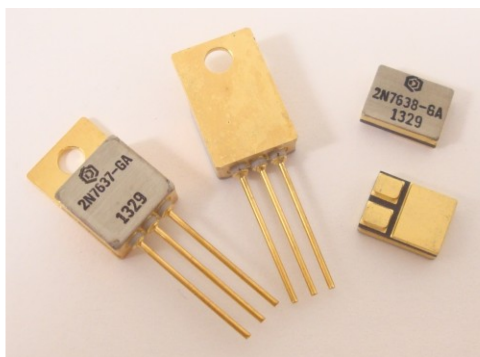

Figure 1: Photographs of 650 V SiC SJTs packaged in 250°C-rated TO-257 and TO-276 headers

RESULTS AND DISCUSSION

Static Characteristics of SiC SJTs

Purely majority-carrier like output characteristics with near-∞ Early voltage are observed in the output characteristics (see Figure 2a) of a 24 mΩ (4 mΩ-cm^2) SiC SJT, packaged in a high-temperature TO-258 header. The β in the active region is as high as 105-111 for drain current in the range of 40 A – 90 A. The current gain shows an expected negative temperature co-efficient (Figure 2b) due to the increasing ionization of Al acceptors in the base layer. However, a β as high as 70 is observed at 250°C. The on-resistance shows a positive temperature co-efficient, which is typical for SiC SJTs.

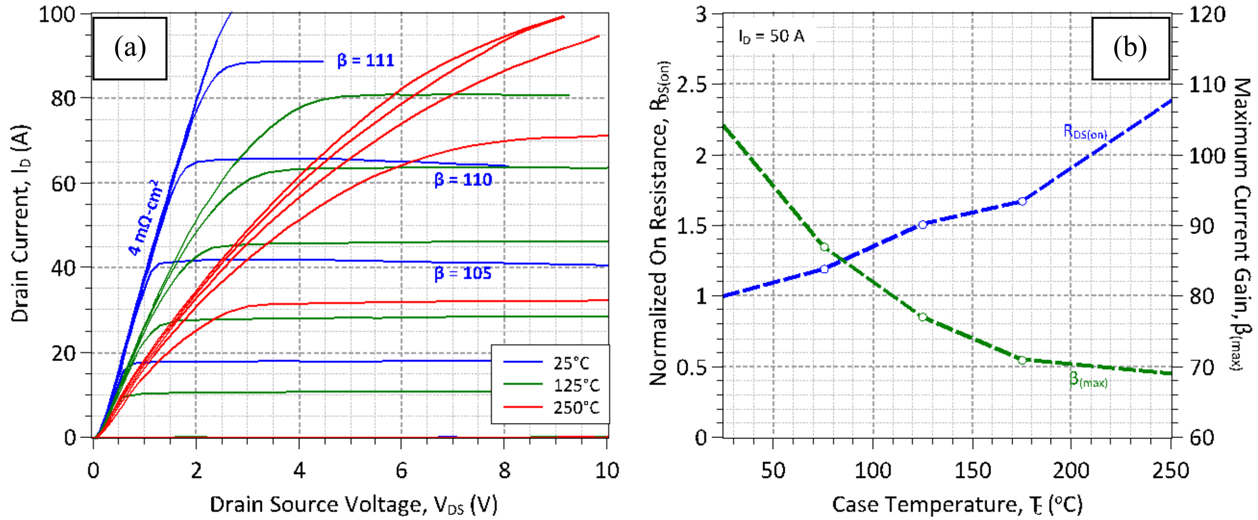

Figure 2 (a): Output characteristics and (b) Temperature variation of β and Ron of a 650 V/19 mm^2 SiC SJT (active area = 17.4 mm^2). This SJT part has a 50 A current rating.

The high-voltage blocking I-V characteristics measured on a 650 V/50 A SiC SJT at different temperatures is shown in Figure 3. Extremely low leakage currents < 1 mA/cm^2 are measured at the rated 650 V, even at temperatures as high as 250°C, indicating the robustness of the edge termination scheme used for device fabrication.

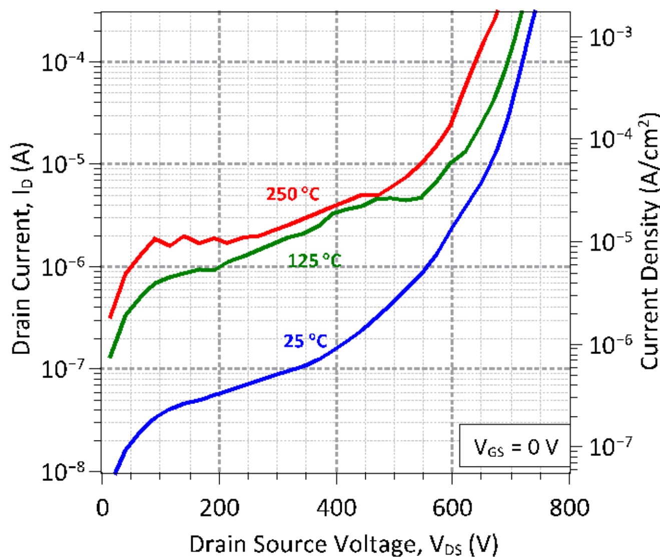

Figure 3: Blocking I-V characteristics measured on a 650 V/19 mm^2 SiC SJT up to 250°C.

While current gains as high as 257 were reported [2] on single-finger test BJTs, the devices reported in this paper show the highest current gain ever recorded on a multi-ampere

power transistor, which also display robust blocking voltages > 600 V. The variation of β at extremely high drain current densities (up to 2000 A/cm^2) was investigated by single 3 μs-wide, 10 Hz pulsed current measurements on 3.5 mm^2 SJTs (Figure 4) to minimize any device self-heating. The current gain is relatively flat up to 800 A/cm^2 at all temperatures, indicating a low surface recombination velocity. The knee-current above which the β rolls off steeply reduces from 1700 A/cm^2 at 25°C to about 800 A/cm^2 at 175°C, from which the safe-operating area for high pulsed current SJT operation can be inferred. The electron mobility decreases with increasing temperature, which in turn increases the voltage drop across the low doped n- drift layer for a fixed drain current. This increased voltage drop causes the p-base/n- layer to become forward biased at a lower drain current at high temperatures, thereby lowering the knee current for β roll-off.

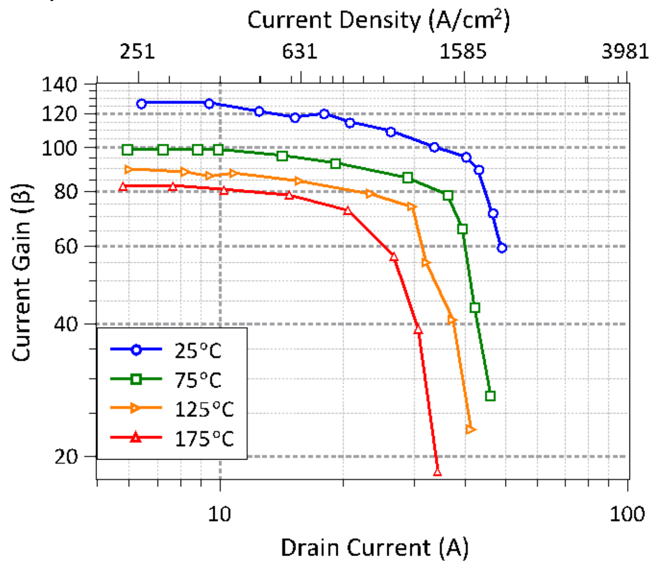

Figure 4: Current gain of a packaged 3.5 mm^2 SiC SJT at ultra-high current densities investigated by pulsed current measurements at various temperatures. Note that these knee currents are significantly lower than the threshold current for the onset of the Kirk effect, which is calculated as 14.3 kA/cm^2 using the SiC material and SJT epitaxial parameters

Static Characteristics of 250°C capable SiC Schottky Rectifiers

The reverse bias I-V characteristics measured on a 1200 V/5 A high-temperature Schottky rectifier are shown in Figure 5a. Reverse leakage currents less than 30 μA and a positive temperature co-efficient are observed in the blocking I-V characteristics, a clear signature of avalanche breakdown. While GeneSiC's standard line of 1200 V Schottky rectifiers offer the lowest leakage current among competing devices (Figure 5b), the special low-leakage process used for GeneSiC's high-temperature or SHT rectifier results in a further 27% reduction in leakage current at 175 °C, as compared to GeneSiC's standard Schottky rectifier.

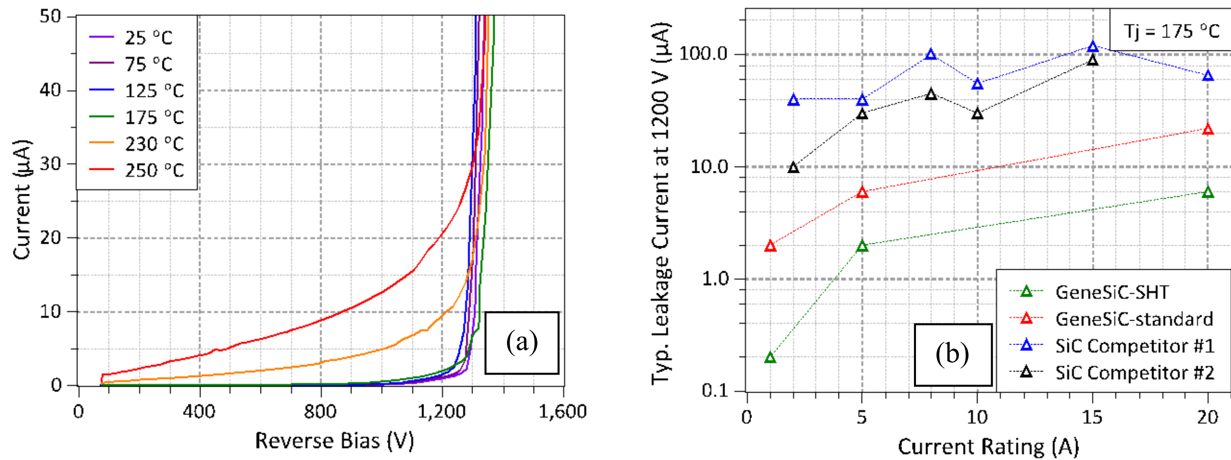

Figure 5 (a): Reverse Bias I-V characteristics measured on a 1200 V/ 5 A SHT rectifier up to 250°C and (b): Comparison of typical leakage currents measured on several 1200 V-class GeneSiC and competitor SiC Schottky rectifiers.

Long-term HTRB on Schottky rectifiers

About 77 packaged parts from GeneSiC's 1200 V/3 A SiC Schottky rectifier line were subjected to 128 hour long, industry-standard high-temperature reverse bias (HTRB) stressing at an elevated temperature of 175°C, in order to identify any potential device degradation pathways. The HTRB stressing was simultaneously performed on all 77 packaged rectifiers at a reverse bias of 960 V. The cumulative reverse leakage current was continuously monitored during this test and shows excellent stability over the entire course of the test duration. A shift analysis performed after the conclusion of the HTRB test yielded an average increase of 5.5% in the breakdown voltage, with a standard deviation of 1.9%, after the 128-hour HTRB stress.

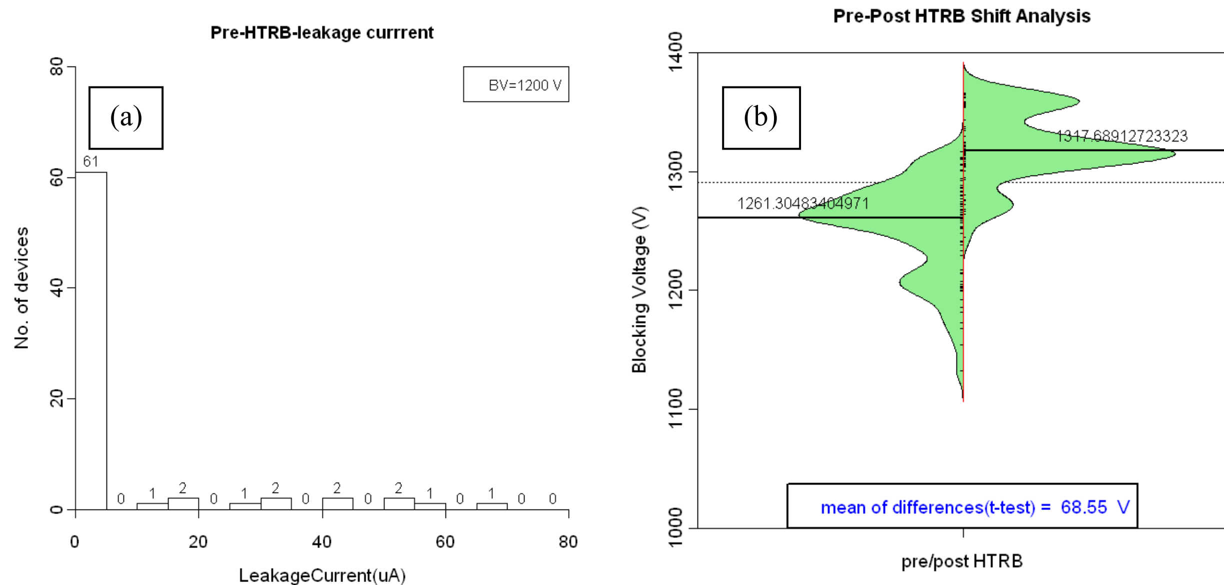

Figure 6 (a): Histogram of leakage currents measured at 1200 V and 25°C on 77 Schottky rectifiers prior to a 128-hour HTRB stress test performed at 960 V, in a 175°C oven. (b): A two-sided bi-variate box plot showing a mean increase of 68.6 V in the breakdown voltage after 128 hours of 175°C HTRB stress. No device failures were noted as a result of HTRB stressing.

Long-Term HTRB on SiC SJTs

About 19, 1200 V/6 A SiC SJTs were subjected to a 336-hour HTRB stress at V_{DS} = 960 V (V_{GS} = 0 V) in a 175°C oven. The breakdown voltage was extracted from pre- and post-stress I-V measurements. A mean drop of 17 V was observed in the breakdown voltage after the 336 hour HTRB stressing. The current gains of these early-stage SJTs also remained fairly stable after the long-term HTRB stress.

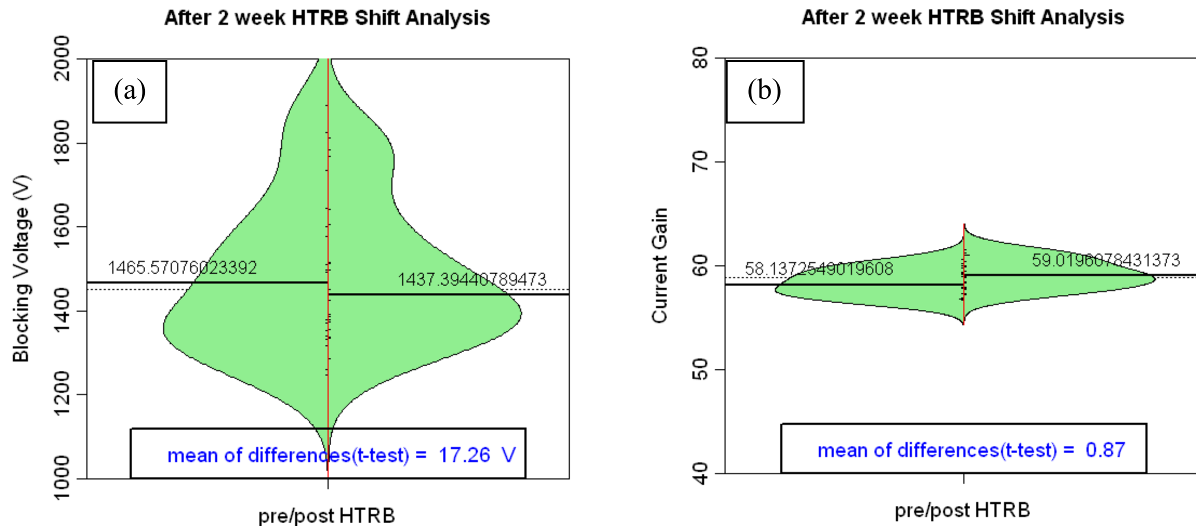

Figure 7: Two-sided bi-variate box plots of the (a) blocking voltage and (b) current gain measured before and after a 336 hour long HTRB stress applied to 19, 1200 V/6 A SiC SJTs at a V_{DS} = 960 V, in a 175°C oven.

SJT Current Gain Stability

Low to moderate current gain (β) degradation is typically observed when current-controlled SiC transistors (SJTs or BJTs) are subjected to long-term high-current operation, specifically at elevated junction temperatures (T_J). SiC BJTs or SJTs fabricated even on basal plane dislocation (BPD)-free material are not immune from β degradation, which is attributed to charge trapping by recombination centers in the p-type base layer close to the SiC surface. Early stage SiC SJTs displayed a 25% compression of the current gain [3], when subjected to a 25-hour stress with DC drain current of 200 A/cm^2, at a $T_J \approx$ 125°C. Subsequent improvements to the SJT device design and process have significantly alleviated the β compression, in addition to increasing the absolute values of the current gain. Recently fabricated SJTs under a similar DC current stress at $T_J \approx$125°C show only a 9-13% β reduction in over 190 hours of testing. Preliminary testing (not shown) indicates that when a short burn is performed at room-temperature, the β stability of these devices appears to be further enhanced. A detailed report of these findings will be published elsewhere.

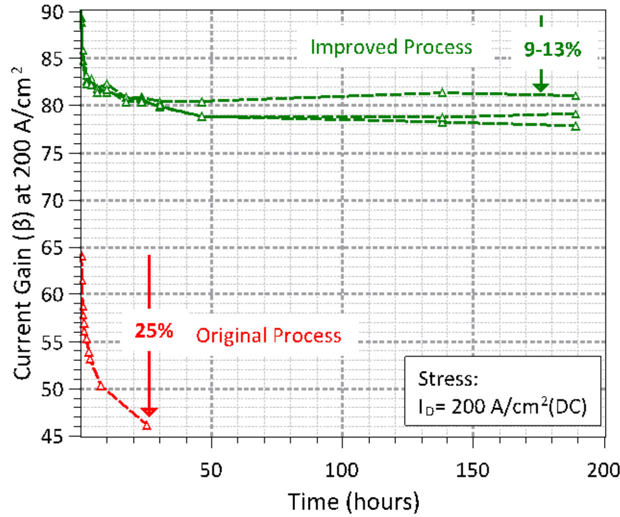

Figure 8: Current Gain (β) stability of SiC SJTs fabricated with the original and improved process under a 200 A/cm^2 DC current stress at an estimated junction temperature of 125°C.

REFERENCES

[1] S. Sundaresan, R. Singh, R.W. Johnson, "Silicon Carbide Junction Transistors operating at 500°C", in proceedings of IMAPS High Temperature Electronics Conference (HiTEC), May 8-10, 2012, Albuquerque, NM, pp. 162-166

[2] H. Miyake et al. "4H-SiC BJTs with record current gains of 257 on (0001) and 335 on (000-1), Electron Dev. Lett. 32(7), pp.841-843 (2011).

[3] S. Sundaresan, A-M Soe, S. Jeliazkov, R. Singh, "Characterization of the stability of the current gain and avalanche mode operation of 4H-SiC BJTs", IEEE Trans. Electron Dev. 59(10), pp.2795-2802 (2012).