Characterization of the Stability of Current Gain and Avalanche-Mode Operation of 4H-SiC BJTs

Siddarth G. Sundaresan, Aye-Mya Soe, Stoyan Jeliazkov, and Ranbir Singh, *Member, IEEE*

***Abstract*—The stability of the electrical characteristics of SiC n-p-n bipolar junction transistors (BJTs) is investigated under long-term avalanche-mode, dc, and pulsed-current operation. There is absolutely no change in the blocking I–V characteristics after a 934-h repetitive avalanche stress test. Long-term operation of the base–emitter diode (open-collector mode) alone does not result in any degradation of the ON-state voltage drop V_F or current gain β. Long-term operation in common-emitter mode results in negligible V_F or β degradation, if the base plate is maintained at 25 °C. A greater degradation of β results upon increasing the base-plate temperature. The same total electrical charge, if passed through the BJT as a pulsed current, instead of a dc current, results in smaller β reduction. It is also shown that the β degradation can be reversed by annealing at $\geq$ 200 °C, suggesting the possibility of degradation-free operation of SiC BJTs, when operating in pulsed current mode at $\geq$ 200 °C temperatures.**

***Index Terms*—Avalanche breakdown, bipolar junction transistor (BJT), electrical properties, long-term reliability, silicon carbide (SiC) devices.**

I. Introduction

SILICON carbide (SiC) n-p-n bipolar junction transistors (BJTs) are developed by GeneSiC with 1200-V to 10-kV ratings. 1200-V/5-A-rated SiC BJTs with current gains β as high as 88 and ultrafast switching times of $<$ 15 ns were recently reported [1]. In this paper, a comprehensive evaluation of the stability of the BJT current gain β after long-term operation is presented. The stability of the leakage currents in blocking mode after single-pulse and repetitive forced-avalanche-mode operation of the SiC BJTs are also investigated.

There are several publications that discuss the stability of the current gain (β) and ON-state voltage drop (V_F) of SiC BJTs, when the devices are subjected to long-term open-collector or common-emitter operation. These reports contain conflicting results ranging from near-perfect β and V_F stability to significant gain compression. A simulation-focused study [2] attributed the cause for the observed current gain compression in SiC BJTs to electrical carrier traps in the base–emitter space charge region or in the bulk of the quasi-neutral base layer. Another study [3] ascribed the current gain compression to basal plane dislocations (BPDs) in the base and/or collector regions. Ghandi *et al.* reported [4] significant current gain degradation for 3-mm^2 SiC BJTs but nearly stable β for smaller area (0.04 mm^2) devices, when the devices were subjected to long-term operation. However, an open-collector bias was used to stress the small devices, whereas the large-area devices were subjected to common-emitter mode operation. Zhang *et al.* [5] reported that a 150-A/cm^2 dc collector current stress applied for 45–78 h resulted in a reduction in β, only above collector current densities of 150 A/cm^2. However, the starting current gain of the stressed SiC BJT in this study was only 35, which makes it difficult to compare their results with the high-gain $(\beta > 70)$ BJTs used in this study.

Therefore, a key focus of this work is an attempt to resolve these conflicting reports by examining the stability of β and V_F of SiC BJTs under various long-term operating conditions including dc or pulsed-current regimes and at actively controlled case temperatures ranging from 25 °C to 125 °C.

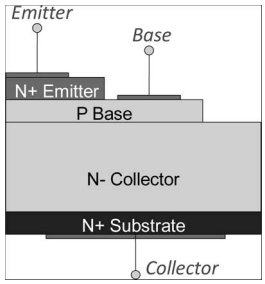

Fig. 1. Simplified cross-sectional schematic of the n-p-n SiC BJT device structure explored in this work. A 12 μm/8 $\times$ 10^{15} cm^{-3} n-collector layer was used, whereas the thickness and doping concentrations of the emitter and base layers was carefully designed for optimizing the ON-state characteristics of the BJTs.

II. Experimental

Several 1200-V/5-A-rated SiC BJTs (active area = 2.97 mm^2) fabricated and packaged in test coupons at GeneSiC were used for performing the reliability characterization for this study. A simplified cross-sectional schematic of the SiC BJTs investigated in this study is shown in Fig. 1.

For the long-term stability investigations of the BJT ON-state characteristics, a custom-designed test bench consisting of an active temperature-controlled hotplate was used to maintain a constant base-plate temperature during long-term operation of the devices. The BJTs were triggered by an off-the-shelf Si insulated gate bipolar transistor (IGBT) gate driver. A 100-nF dynamic capacitor connected in parallel with a 22-Ω gate resistor provided high transient currents for fast sub-20-ns BJT switching. For the forced-avalanche-mode tests, an unclamped inductive load test setup was used. The carrier lifetime in the

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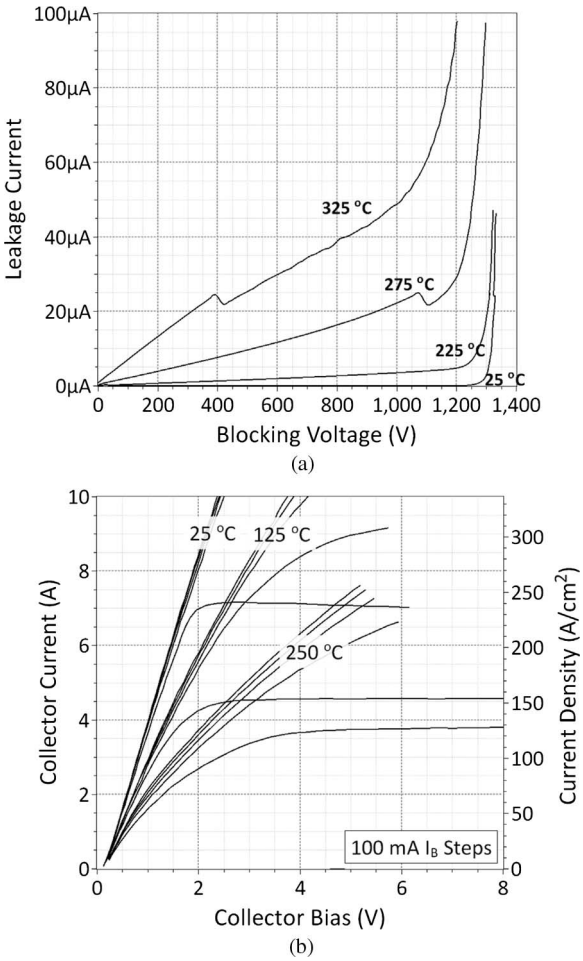

Fig. 2. (a) Open-base blocking I–V characteristics measured on a 1200-V/5-A BJT up to 325 °C. (b) Output characteristics of a 1200-V/5-A BJT measured up to 250 °C.

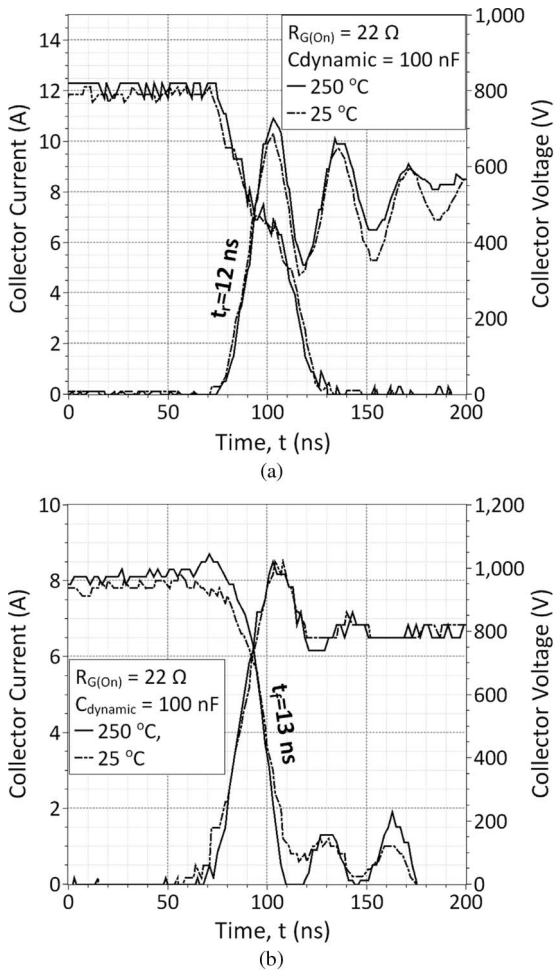

Fig. 3. (a) Turn-on and (b) turn-off collector current and voltage transients recorded for switching 800 V and 8 A through a 1200-V/5-A SiC BJT. There is no difference in switching speed between 25 °C and 250 °C, due to the "unipolar" nature of the SiC BJT device design.

BJT base layers was measured by the open-circuit voltage decay (OCVD) technique [6].

III. Results and Discussion

A. Static I–V Characterization

Optimized BJT process design and fabrication were used to realize near-theoretical breakdown voltages and low leakage currents up to 325 °C [Fig. 2(a)]. The output I–V characteristics of a 1200-V/5-A SiC BJT shown in Fig. 2(b) feature a near-zero collector–emitter offset voltage, distinct lack of a quasi-saturation region, and merging of the different base current I–V curves in the saturation region. The last two features imply lack of minority carrier charge storage in the collector region of the SiC BJT and clearly distinguishes this device from a "bipolar" Si BJT. This inherent property of the SiC BJT enables temperature-invariant fast-switching transients. Appropriate metallization schemes along with an optimized epilayer design resulted in $V_{\mathrm{CE,SAT}}$ values at a collector current of 5 A as low as 1.15 V at 25 °C and 2.8 V at 250 °C. The positive temperature coefficient of on-resistance observed in Fig. 2(b) is desirable for paralleling multiple devices for high-current configurations, without risk of thermal runaway.

B. Switching Characterization

Switching measurements of the 5-A SiC BJTs were performed with an inductive load and free-wheeling 1200-V/7-A SiC Schottky rectifiers, also fabricated at GeneSiC. A commercially available IGBT gate driver with an output voltage swing from −8 to 15 V was used for driving the BJTs. A 100-nF dynamic capacitor connected in parallel with the base resistor generated high initial dynamic base currents of 3.5 and −1 A during turn-on and turn-off, respectively, while maintaining a constant base current of 0.52 A during the on pulse. These large dynamic base currents charge/discharge the device input capacitance rapidly, yielding a faster switching performance. Temperature-invariant ultra-low collector current rise and fall times of 12 and 13 ns, respectively, were recorded (Fig. 3) for switching 8 A and 800 V through the SiC BJT.

C. Avalanche Ruggedness

Previously [1], a single-pulse avalanche energy rating (E_{AS}) of 20.4 mJ and an avalanche voltage of 1500 V were measured by unclamped inductive switching (UIS) of a 1200-V/5-A-rated SiC BJT. 1200-V/20-A-rated SiC DMOSFETs with

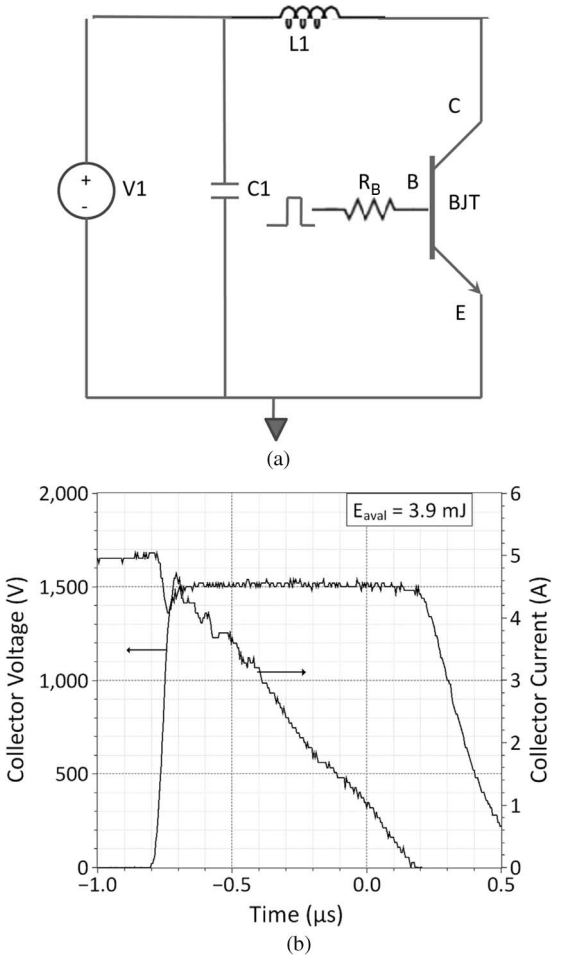

Fig. 4. (a) Unclamped inductive load circuit used for driving the SiC BJTs into avalanche mode. (b) Example waveform of a 1200-V/5-A SiC BJT dissipating 3.9 mJ under avalanche-mode conditions. The device turns off 5 A (168 A/cm^2) of current, when biased at an avalanche voltage of 1500 V by the unclamped inductive load of 0.31 mH. A constant base current of 250 mA was applied to turn on the device.

$E_{\rm AS} = 500$ mJ have been reported [7]. The significantly higher $E_{\rm AS}$ reported in [7] could be due to the SiC DMOSFET's significantly larger chip size (9.6 mm^2), higher avalanche voltage (2100 V), and more planar structure in comparison with the SiC BJTs fabricated in this study.

In this paper, the stability of the blocking I–V characteristics after both single-pulse and repetitive avalanche regime operation is investigated. The circuit used for performing UIS testing of the BJTs is shown in Fig. 4(a). A constant base current of 0.25 A was applied for turning-on the BJTs to their rated 5 A (168 A/cm^2), and the value of the inductor L1 $= 0.31$ mH was adjusted to achieve a fixed turn-off time (hence avalanche energy).

A 1200-V/5-A SiC BJT was subjected to five 3.9-mJ pulses in the avalanche regime [see test waveforms in Fig. 4(b)], and the blocking I–V characteristics were measured after each test (not shown). There was no change in the blocking characteristics of the BJT before and after the application of the avalanche-mode pulses.

In a separate experiment, another device was subjected to repetitive 2.3-mJ avalanche-mode pulses with a frequency of

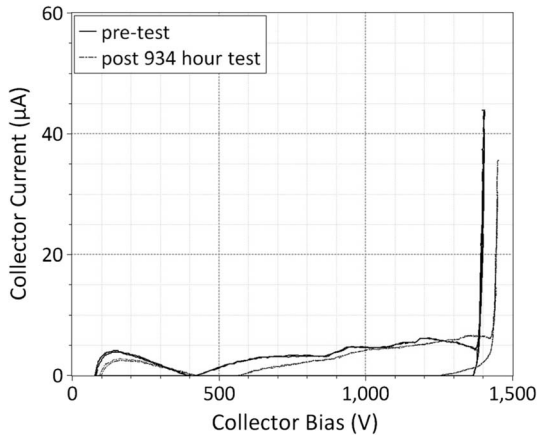

Fig. 5. Examination of the (open-base) collector–emitter blocking characteristics of a 1200-V/5-A SiC BJT before and after repetitive avalanche stress was applied to the device for 934 h.

14.3 kHz, a duty cycle of 30%, a base current of 0.25 A, and a collector current of 5 A. This test was run for 934 h. The blocking I–V characteristics measured before and after this long-duration test (Fig. 5) indicated a slight improvement of the breakdown voltage from 1400 to 1450 V, after 934 h of operation under avalanche mode.

These results indicate that the SiC BJTs reported in this study offer stable operation, even after long-term avalanche-mode operation at high current densities. This feature clearly distinguishes them from Si BJTs, in which the collector currents need to be significantly derated when operating at high collector biases, due to the second breakdown effect [8], [9].

D. Stability of Current Gain and on-*State Voltage Drop After Long-Term Operation*

In this paper, a comprehensive set of experiments is performed to better understand the long-term stability of the ON-state characteristics of the SiC BJTs, specifically the current gain (β) and V_F. A series of long-term operation tests with varying base-plate temperature and on-pulse duration (duty cycle) are performed. The devices are either stressed by dc or pulsed currents. All the dc current tests are performed for an arbitrarily chosen total duration of 5.8 h. For all the pulsed current tests, the exact same base driving scheme used for the obtaining the switching waveforms in Fig. 3 was employed. Representative base voltage/current waveforms are shown in Fig. 6, which indicate a peak turn-on base current of 3.5 A, a steady-state base current of $\sim$0.5 A, and a peak turn-off base current of -1.2 A.

The current gain β is always calculated at room temperature, at the rated collector current of 5 A, at $V_{\rm CE} = 10$ V (in the active region) for the BJTs investigated in this study. All devices selected for these experiments had a pretest β in the range of 68–72. For reference, the theoretical or "intrinsic" current gain β_T for the SiC BJTs reported in this work, only limited by the base transport factor is calculated as 162, using the carrier-concentration-dependent electron mobilities and minority carrier lifetimes from [10].

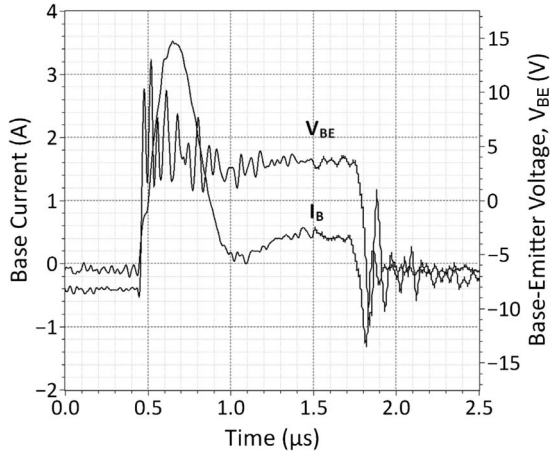

Fig. 6. Representative base current/voltage waveforms used for pulsed current stressing of the SiC BJTs in this study.

1) Influence of Base-Plate Temperature: A set of long-term dc operation tests with a constant collector current of 5 A and a constant base current of 250 mA was performed on several 1200-V BJTs, at base-plate temperatures ranging from 25 °C to 125 °C. The devices were continuously biased for 5.8 h, and the ON-state characteristics were periodically obtained by interrupting the tests and cooling the devices down to room-temperature, from which β and V_F were extracted.

The evolution of β versus test duration is shown in Fig. 7(a), where it can be clearly seen that stressing the devices at a higher base-plate temperature resulted in greater reduction in β. This indicates that the carrier-trapping mechanism responsible for current gain reduction is more efficient at higher junction temperatures. From Fig. 7(a), a negligible β reduction (from 68.5 to 66) after 5.8 h of dc operation is obtained, when the base-plate temperature is maintained at 25 °C. However, a significant β reduction from 69.4 to 52 is observed in 5.8 h, when the base-plate temperature is increased to 125 °C. A comparison of the BJT output characteristics at room-temperature, before and after the 5.8-h dc bias test performed at a base-plate temperature of 25 °C [Fig. 7(b)] reveals no change in the device on-resistance after the test. On the other hand, the 5.8-h dc test at a base-plate temperature of 125 °C results in a finite increase in V_F by 300 mV at a collector current of 5 A [Fig. 7(c)]. It is important to point out that no distinct quasi-saturation region can be observed in the post-stress output characteristics [Fig. 7(b) and (c)]. According to Konstantinov *et al.* [3], the absence of a quasi-saturation region in the post-test characteristics indicates that the observed V_F increase is not due to carrier trapping by BPDs in the lightly doped n-drift layer.

2) DC Versus Pulsed Current Long-Term Operation: It was reported in [11] that the same charge passing through a SiC PiN diode as a dc or pulsed current causes fundamentally different V_F shifts, with the pulsed current causing smaller V_F shifts than the dc current. In this paper, selected SiC BJTs were subjected to long-duration, 5-A dc, or pulsed currents, applied with a pulsewidth of 30 μs and at a switching frequency of 14.3 kHz and at a case temperature of 125 °C. The impact of dc and pulsed-mode operation is compared by plotting the evolution

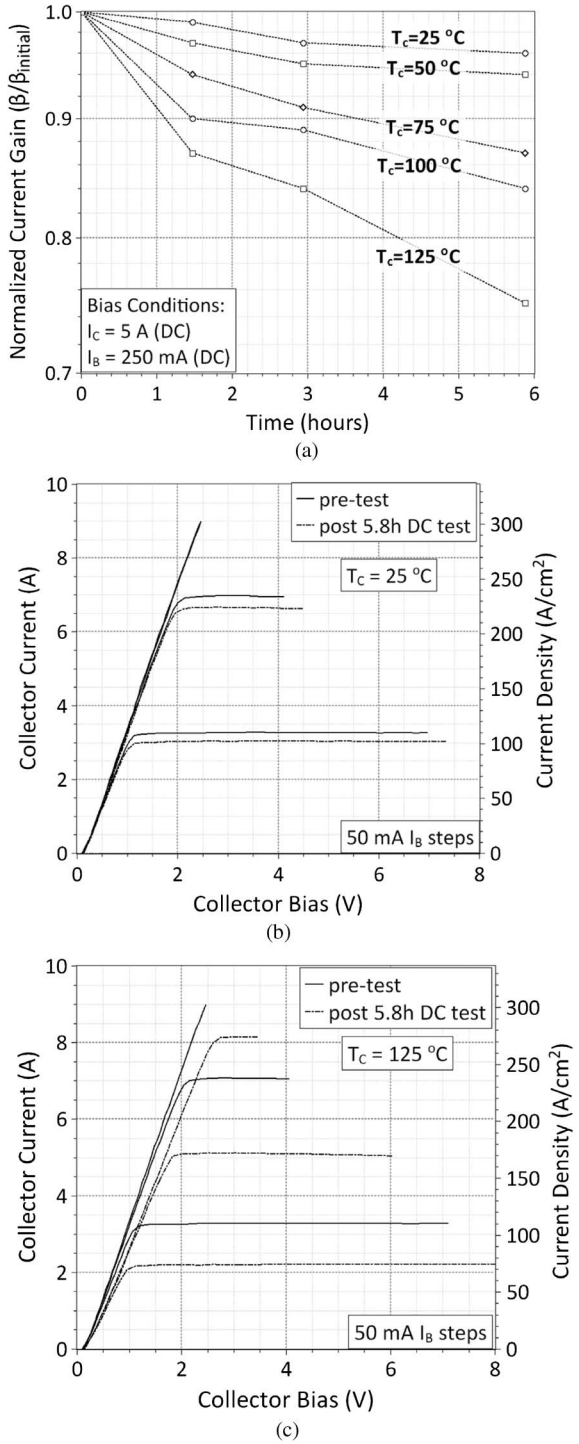

Fig. 7. (a) Variation of the normalized current gain β after long-term dc operation at various base-plate temperatures. (b) BJT output characteristics before and after the long-term dc bias at $T_C = 25$ °C. (c) BJT output characteristics before and after the long-term dc bias at $T_C = 125$ °C.

of β versus the total charge impressed upon the device as the ordinate axis in Fig. 8. The β reduced to 82% of its pretest value after a 15.9-h pulsed-current test, whereas the 5.9-h dc-current test reduced β to 75% of its pretest value, even though the same total charge (106 kC) was impressed on the device during the two tests. This result is consistent with the smaller V_F shift observed under pulse mode versus dc mode [11] for SiC PiN diodes. Additional long-term operation tests

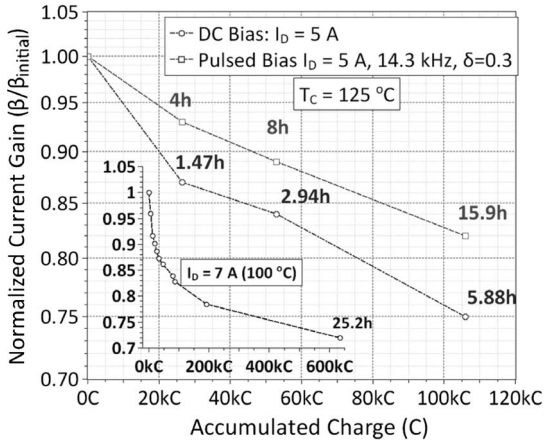

Fig. 8. Variation of normalized BJT current gain (β) after passing 5 A of collector current either as a dc current or as a pulsed current. (Inset) The BJT current gain asymptotically approaches a steady-state value after passing a dc collector current of 7 A at a case temperature of 100 °C for 25.2 h.

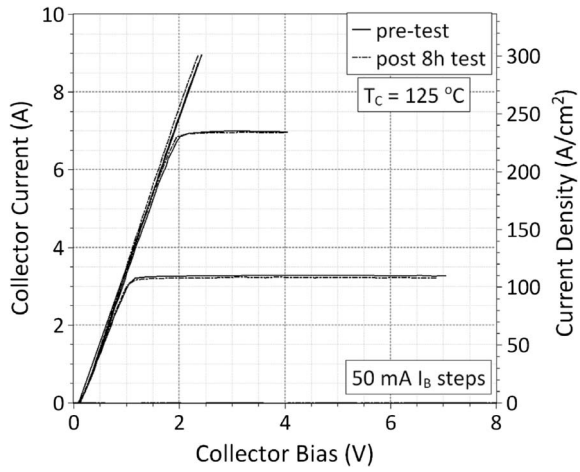

Fig. 9. No current gain or V_F degradation observed in the SiC BJT output characteristics measured before and after 8 h of an open-collector pulsed current test conducted at a frequency of 14.3 kHz, duty cycle of 30%, and base-plate temperature of 125 °C.

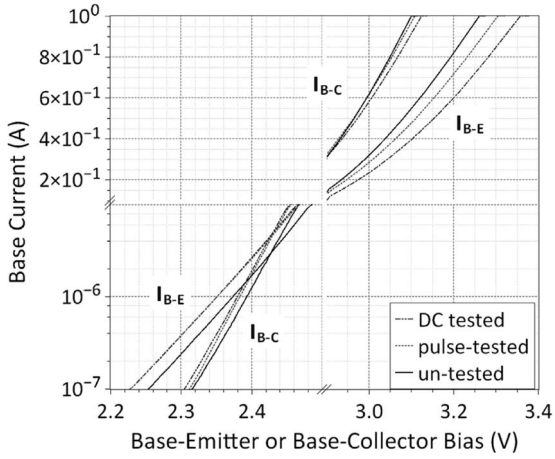

Fig. 10. Base–emitter and base–collector I–V characteristics obtained after passing 106 kC of charge through SiC BJTs, either as dc and pulsed currents, at a base-plate temperature of 125 °C. An increase of base current in the subthreshold region and a decrease of base current in the higher current portion are observed after the long-duration stressing.

(not discussed in this paper for brevity) included varying the duty cycle from 9% to 30% at a fixed frequency of 14.3 kHz. Increasing the on-pulse duration resulted in greater β reduction. Along with the increased gain reduction observed at higher base-plate temperatures [Fig. 7(a)], it is clear from these tests that the total charge passing through the SiC BJT is not the only parameter in determining the amount of current gain reduction. The junction temperature, at which the device is operated, appears to play a critical role in determining the amount of current gain compression.

In a separate experiment (shown as an inset in Fig. 8), another device was stressed by passing 7 A of dc current in the common-emitter mode, at a base-plate temperature of 100 °C. After running this test for 25.2 h, it can be clearly seen that the current gain asymptotically approaches a steady-state value, which, in this instance, corresponds to ∼70% of its pretest value. This is an important result, which shows that the current gain of the SiC BJTs fabricated in this work can, in fact, be stabilized by a long-duration burn-in.

3) Long-Term Open-Collector Operation: It was suggested using device simulations in [2] that carrier traps either in the bulk of the base layer or at the base–emitter space-charge region may be responsible for gain compression in SiC BJTs. Konstantinov *et al.* [3] observed that long-term open-collector mode operation alone resulted in current gain compression of SiC BJTs. Lindgren *et al.* from the same group, in a later publication [12], showed degradation-free I–V characteristics for a 18.4-mm^2 SiC BJT after a 660-h open-collector test at a dc base current of 250 mA.

In this paper, long-term (8 h) pulsed testing of the base–emitter diode of a SiC BJT (or open-collector operation) was conducted at a duty cycle of 30% and at a switching frequency of 14.3 kHz. The same base drive (see Fig. 6) used for the previously described tests was employed. The base-plate temperature was maintained at 125 °C to enhance the gain degradation, if any. Fig. 9 shows absolutely no reduction in β after the 8-h open-collector pulsed-current test. In contrast, β decreased to 89% of its initial value, when a BJT was subjected to 5-A collector current pulses in the common-emitter mode for the same duration (8 h), with the same base drive, duty cycle, frequency and base-plate temperature [see Fig. 8]. This finding is in agreement with the results reported by Lindgren *et al.* [12], who observed no current gain degradation after an open-collector long-term stress.

Factors Responsible for Current Gain Reduction: From the results reported in Figs. 7 and 8, it is clear that a greater current gain reduction over time is possible by (A) increasing the base-plate temperature and (B) operation at wider pulse widths and lower operating frequencies. According to this line of reasoning, the invariance of current gain observed after the open-collector test in Fig. 9 may be due to a lower junction temperature of the device, due to the passage of lower currents in comparison with the common-emitter test.

The base–emitter and base–collector I–V characteristics were examined after passing 106 kC of charge through two BJTs as dc and pulsed currents, respectively (Fig. 10).

After the long-term stresses, the base current of the base–emitter diode shows a marked increase in the subthreshold region, indicating an increase to the recombination component of the base current. Interestingly, there is no difference in the

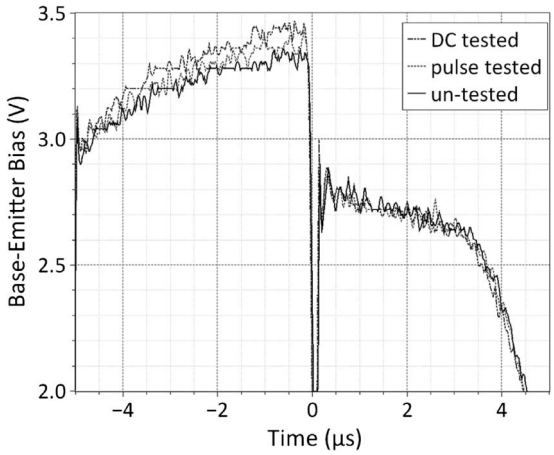

Fig. 11. Voltage decay waveforms from OCVD measurements of the base–emitter p-n junction of SiC BJTs, stressed by passing 106 kC of charge as long-term dc and pulsed current operation, at a base-plate temperature of 125 °C. The overlapping of the curves in both the linear and nonlinear portions of the voltage decay indicates no change to the high-level and recombination carrier lifetime in the bulk of the base layer.

subthreshold base–emitter I–V characteristics between the devices stressed by dc and pulsed currents, even though the dc current stress created a greater (25%) β reduction (see Fig. 8) than the pulsed current stress (18%). In the higher current (> 0.1 A) portion of the base–emitter I–V characteristics, a greater base current reduction is observed after the dc current stress in comparison with the pulsed current stress. The increased base resistance after long-term electrical stressing could explain the 300 mV increase of V_F observed in Fig. 7(c) after the long-term DC bias test.

The different impact of the dc and pulsed current stressing on the low- and high-current portion of the base–emitter I–V curves imply that there could be more than one physical mechanism responsible for the observed β reduction. Compared to the base–emitter I–V characteristics, the base–collector diode shows a significantly lower current increase in the subthreshold region, indicating that the carrier recombination centers responsible for β reduction are located in the vicinity of the base–emitter junction region of the SiC BJT, close to the SiC surface.

To investigate any correlation between β reduction and high-level carrier lifetime (t_{HL}) in the base layer, OCVD measurements were performed on the base–emitter p-n junction of devices stressed by long-term dc and pulsed currents. These are the same devices reported in Fig. 10. The voltage decay waveforms are obtained by turning-off a base current of 1 A at $t = 0$, in Fig. 11.

Both the linear and nonlinear portions of the voltage decay waveforms in Fig. 11 are overlapped for the unstressed, dc, and pulsed-current stressed devices. From the slope of the linear portion of the voltage decay waveforms, a high-level carrier lifetime of 870 ns is extracted. The overlapping of the nonlinear voltage decay portion of the OCVD waveforms indicates no change in the low-level (or recombination) carrier lifetime in the base layer as well, after the long-term operation tests. Since the OCVD technique measures the carrier lifetime in the bulk of the base layer [6], this finding implies that carrier traps responsible for β reduction are not located in the bulk of the base layer but rather at the base–emitter junction interface with the dielectric passivation layer. The higher junction temperatures resulting from operating the BJT at either a higher base-plate temperature or a higher duty cycle increases the capturing efficiency of these traps, which results in greater current gain compression. The results presented in this study also suggest that the positive V_F shift observed after stressing the SiC BJTs is associated with the reduced emitter injection efficiency of the base–emitter p-n junction and is not due to the presence of BPDs in the lightly doped n-drift layer, as observed by Konstantinov *et al.* [3].

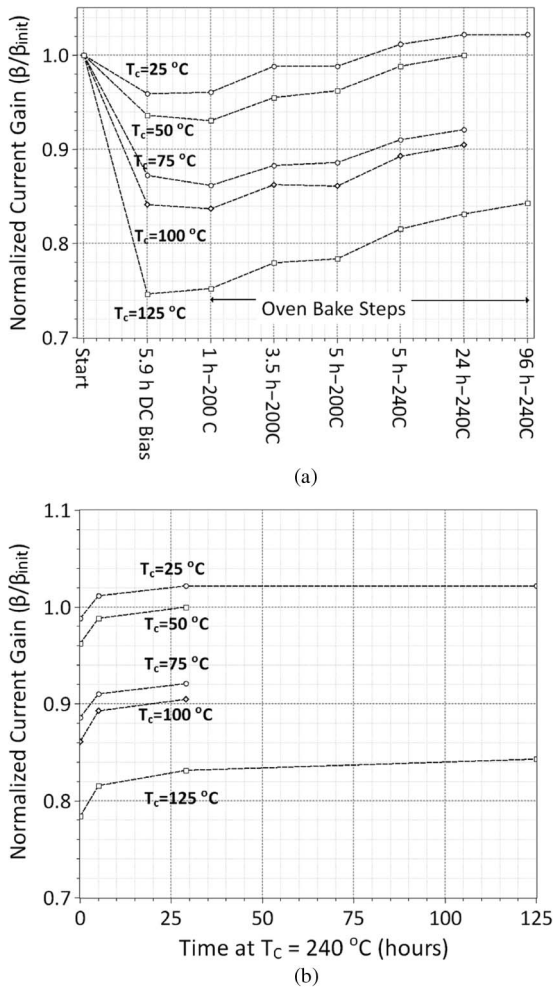

Fig. 12. (a) Current gain recovery of SiC BJTs subjected to long-term dc current stress tests achieved by baking in a temperature controlled oven. (b) Time dependence of the current gain recovery process at a temperature of 240 °C.

E. Current Gain Recovery by Thermal Annealing

There are reports [13], [14] indicating that the V_F shift caused by long-term operation of SiC PiN and Merged PiN Schottky (MPS) diodes can be recovered by thermal annealing in the range of 300 °C–400 °C for several hours. To investigate possible recovery of the current gain, the SiC BJTs subjected to long-term operation at various base-plate temperatures in this work [see Fig. 7(a)] were later subjected to various sequential annealing treatments at 200 °C and 240 °C, in a temperature-controlled oven [Fig. 12(a)].

As shown in Fig. 12(a), it can be seen that all previously degraded devices show a current gain recovery upon thermal annealing. Similar to current gain deterioration, the β recovery appears to be temperature dependent from the results shown in Fig. 12. There appears to be a maximum possible recovery of β at a given temperature. After 4.5 h of annealing at 200 °C, a further 5-h annealing at the same temperature did not further recover the current gain. However, β recovers further after a subsequent 240 °C/5-h annealing. Packaging limitations precluded annealing the BJTs at temperatures higher than 240 °C. Interestingly, the β of mildly degraded devices (subjected to 25 °C and 50 °C case temperature stress tests) are even slightly higher than their corresponding pretest values, after the thermal treatment.

F. In Situ Recovery of Current Gain

The experimental results presented in this paper create an intriguing prospect for *in situ* recovery of the current gain of SiC BJTs by operating them in the pulsed mode at high ($\geq$ 200 °C) ambient temperatures. It is possible that any β or V_F degradation occurring during the on-pulse could be recovered during the off-pulse, provided the off-pulse is long enough for complete recovery. Long-term electrical stressing of SiC MPS diodes PiN diodes at 242 °C [13] and SiC PiN diodes at 200 °C [14] resulted in recovery rather than degradation of V_F. Further tests need to be performed to investigate long-term SiC BJT operation under these high ambient temperature conditions.

IV. Conclusion

A comprehensive evaluation of the reliability of the ON-state and blocking voltage characteristics of SiC BJTs has been presented in this paper. In stark contrast to Si BJTs, the SiC BJTs presented in this study are capable of turning-off high current densities, even under avalanche-mode conditions, with absolutely no change to the blocking I–V characteristics, even after a 934-h repetitive avalanche operation at rated 168 A/cm^2 collector currents. The current gain and V_F are reasonably stable, when the device is operated at 5 A (168 A/cm^2) for several hours at a controlled base-plate temperature of 25 °C. Long-term dc operation at higher base-plate temperatures (up to 125 °C) results in a greater reduction to the current gain and V_F. It was also found that the current gain reduction is significantly smaller, if the same charge is passed through the device as a pulsed current instead of a dc current. Long-term operation of the base–emitter diode alone did not result in any change to the output characteristics. A clear correlation between higher junction temperature and increased level of current gain degradation in SiC BJTs is firmly established by collating these results. It was established through detailed I–V and carrier lifetime characterization that carrier traps at the base–emitter junction interface are responsible for the current gain degradation. It was also shown that the current gain degradation could be at least partially recovered by baking the devices in a temperature controlled oven at 200 °C−240 °C. This raises the possibility of an *in situ* recovery of any degradation of the current gain, by operating the SiC BJTs in pulsed mode at high ($>$ 200 °C) ambient temperatures.

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